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USER'S DESIGN HANDBOOK

FOR

A STANDARDIZED CONTROL MODULE (SCM)

FOR

DC TO DC CONVERTERS

VOLUME II

FINAL REPORT

BY

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16. Abstract

Three basic switching regulators: buck, boost, and buck/boost, employing a Standardized Control Module (SCM) were characterized by a common small signal block diagram in Volume I of the report, "Application Handbook for a Standardized Control Module for DC-DC Converters." Employing the unified model, regulator performance such as stability, audiosusceptibility, output impedance, and step-load transient were analyzed and key performance indices were expressed in simple analytical forms. It has been demonstrated that the performance characteristics of all three regulators are shown to enjoy common properties due to the unique SCM control scheme. This allows simple unified design procedure to be realized in the present report (Volume II) for selecting the key SCM control parameters for an arbitrarily given power-stage configuration and parameter values, such that all regulator performance specifications can be met and optimized concurrently in a single design attempt.

It is the author's intent to make this report (Volume II) be self-contained. For user's convenience, if he (or she) does not wish to go through the detailed modeling and performance analyses as presented in Volume I, all key results and performance indices derived in Volume I which are relevant to SCM design considerations are presented here in Volume II to facilitate frequent references.

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Particularly important to the successful completion of the project was the thorough review from the editor, Mr. Joseph Kolecki, who is also the Project Monitor of NASA Lewis Research Center. His many critical comments had led to substantial improvements during the final revision of this report.

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NOTATIONS

The symbols for currents and voltages at the terminals of devices have subscripts. The uppercase and lowercase symbols and subscripts are used to distinguish between instantaneous values, quiescent values, and small signal low-frequency averaged values.

For example:

v_I : input voltage, instantaneous value

$$v_I \approx V_I + \hat{v}_i$$

V_I : input voltage, dc average value

$\hat{v}_i$: input voltage, small signal low-frequency average term

v_O : output voltage, instantaneous value

$$v_O \approx V_O + \hat{v}_o$$

V_O : output voltage, dc average term

$\hat{v}_o$: output voltage, small-signal low-frequency average term.

T_P : Period of a switching cycle

T_{ON}: Switch on time

T_{F1}: Switch off time in continuous inductor mmf operation

T_{F2}: A portion of the switching off time when the inductor mmf has vanished

d : $\frac{T_{ON}}{T}$ duty cycle ratio $d \approx D + \hat{d}$

D : Steady state duty cycle ratio

$\hat{d}$: Small signal duty cycle variation

d' : $\frac{T_{OFF}}{T_P}$ $d' \approx D' - \hat{d}$

D' : Steady state value for d'

v_C : Output filter capacitor voltage

i_L : Inductor current of the buck and boost converter

ϕ : Magnetic flux of the energy-storage inductor of the two-winding buck/boost converter

$\underline{x} = [i_L, v_C]^T$ state variables for buck and boost converter

$\underline{x} = [\phi, v_C]^T$ state variables for the buck/boost converter

v_{DC} : dc loop sensing voltage $v_{DC} = v_O$

v_{AC} : ac loop sensing voltage

Power Stage

L : energy storage inductor

R_ℓ : winding resistance of L

R_p, R_S : winding resistance of the primary winding and secondary winding, respectively of the two-winding buck/boost converter

C : output filter capacitor

R_C : output filter capacitor ESR

N_L : number of turns of L

N_p, N_S : number of turns for the primary and secondary windings of two winding buck/boost converter

$R_e = R_\ell$ buck

$= R_\ell/(D')^2$ boost

$= R_S/(D')^2$ buck/boost

$L_e = L$ buck

$= L/(D')^2$ boost

$= L_S(D')^2$ buck/boost

$R_{Ce} = R_C$ buck

$= R_C/D'$ boost and buck/boost

$R_{eq} = R_e + R_{Ce} - R_C$

$\omega_o = 1/\sqrt{L_e C}$

$\zeta = \frac{1}{2\omega_o} \cdot \left[\frac{1}{CR_L} + \frac{R_e + R_{Ce}}{L_e} \right]$

$\tau_{Z1} = R_C C$

Control Circuit

R_1, R_2 : control loop resistor divider

R_3 : dc loop resistor

R_4 : ac loop resistor

R_5 : compensation loop resistor

C_1 : operational amplifier integrator capacitor

C_2 : compensation loop capacitor

N_3 : number of turns of the ac sensing winding

n : ac loop sensing winding turns ratio · $n = N_3/N_S$ for buck/boost converter.

$R_x = R_1 \,//\, R_2$

$g = R_2/(R_1 + R_2)$

$$R_y = (R_3 + R_x)/g$$

$$m = R_4/(n\,R_y)$$

$$\alpha = R_4/(n\,R_y) \qquad \text{buck}$$

$$= R_4/(D'n\,R_y) \qquad \text{boost and buck/boost}$$

$$A_1 = 1 \qquad \text{buck}$$

$$= 1 - \frac{R_{eq}}{R_L} + \frac{2\zeta\omega_o L_e}{R_L} - \left(\frac{L_e\omega_o}{R_L}\right)^2 \qquad \text{boost}$$

$$= 1 - \frac{DR_{eq}}{R_L} + \frac{2\zeta\omega_o DL_e}{R_L} - D\left(\frac{L_e\omega_o}{R_L}\right)^2 \qquad \text{buck/boost}$$

$$A_2 = 0 \qquad \text{buck}$$

$$= 1/(R_L C) \qquad \text{boost}$$

$$= D/(R_L C) \qquad \text{buck/boost}$$

$$\tau_{Z2} = (R_5 + R_y)C_2$$

$$\tau_{P1} = R_5 C_2$$

$$\alpha' = \frac{\alpha}{A_1 - A_2\tau_{Z2}\alpha}$$

$$\tau_{z2}' = \tau_{Z2} \qquad \text{buck}$$

$$= \left(\tau_{Z2} + \frac{L_e}{\alpha R_L}\right)\left(1 - \frac{R_{eq}}{R_L}\right) + (1-\alpha)\frac{L_e}{\alpha R_L} \qquad \text{boost}$$

$$= \left(\tau_{Z2} + \frac{L_e}{\alpha R_L}\right)\left(1 - \frac{DR_{eq}}{R_L}\right) + (1-\alpha)\frac{DL_e}{\alpha R_L} \qquad \text{buck/boost}$$

Pulse Modulator:

$$F_M = \frac{2R_4 C_1}{n\,M} \qquad \text{duty cycle modulator gain}$$

M is defined in Table 7-1

Others:

$K_1 = \frac{2V_I}{M}$ buck, $K_1 = \frac{2V_I}{D'M}$ boost, $K_1 = \frac{N_S}{N_p}\frac{2V_I}{DM}$ buck/boost

$K_2 = D$ buck

$= \frac{D}{D'}(1 + \frac{2V_I L_e}{R_L M})$ boost

$= \frac{N_S}{N_p}\frac{D}{D'}(1 + \frac{2V_I L_e}{R_L M} D)$ buck/boost

$\mu = 1/D$ buck

$= D'$ boost

$= (N_p D')/(N_S D)$ buck/boost

System model:

A. Power stage transfer functions $F_I, F_D, F_p, Z_p, F_1, F_2 F_3$ and F_4:

$F_p(s)$: equivalent output filter transfer function

$F_I(s)$: input voltage gain, ($F_I F_p$ represents the open loop input-to-output-voltage transfer function)

$F_D(s)$: duty cycle gain, ($F_D F_p$ represents the duty-cycle-to-output-voltage gain)

$Z_p(s)$: the output impedance of the open-loop converter power stage ($Z_p \hat{i}_o$ represents the open-loop output voltage variation due to the load current disturbance $\hat{i}_o$)

$F_1(s)$ and $F_2(s)$ together provides the small-signal low-frequency ac inductor (or magnetic flux) current due to disturbances from the output voltage $\hat{V}_o$ and duty cycle $\hat{d}$.

$F_3(s)$: Impedance function employed to convert the inductor current or magnetic flux into an ac loop error voltage $V_{ac}(s)$ across the sensing winding.

$F_4(s)$: Transfer function characterizing the amount of disturbance of the inductor current due to load disturbance.

B. Analog signal processor (ASP) transfer functions: F_{DC} and F_{AC}:

$F_{DC}(s)$: the transfer function of the combined dc loop and RC compensation loop.

$F_{AC}(s)$: the transfer function of the ac loop

C. Duty cycle pulse modulator transfer function F_M

F_M : the describing function of the duty cycle pulse modulator

Analytical expression for F's are defined in Table 8-1.

CHAPTER 1

INTRODUCTION

Functionally speaking, a dc-dc regulated converter can be divided into two parts: a power circuit and a control circuit. By definition, the power circuit handles the energy transfer from the source to the load. The control circuit manages the rate of the source-load energy transfer as a function of the load demands. During nominal steady-state and transient operations, the control objectives are associated with (A) the tracking of a certain controlled quantity in accordance with a given reference, and (B) the compliance of converter specifications such as the system response to step or sinusoidal line and load disturbances and to external command signals. During abnominal operations, the control objective becomes the electrical-stress limiting for all elements associated with the converter to provide effective protection against catastrophic/degration types of failures. A control circuit thus serves the multiple functions of regulation, command, and protection.

The electrical performance of dc-dc switching regulators is largely dictated by the particular power stage configuration and control method chosen. Often in the design practice, when a power stage is chosen and parts designed, the subsequent attention is then focused on selecting the best suitable control method and frequency stabilization (compensation) network tailored to the chosen power stage in order to optimize the overall system performances. The lack of a unified control method and design strategy often necessitates the undertaking of time consuming

paper and bench design iterations which frequently result in incompatible and intricate performance characteristics.

The incentive for performance improvement and control standardization had prompted the initial development of a multiple-loop control concept in the late sixties [1]. Since then, the control concept has undergone several major program efforts, which culminate in the development of a Standardized Control Module (SCM) for dc-dc converters [2,3]. Figure 1.1 illustrates the SCM applied to the three basic power stages, buck, boost and buck/boost. The SCM contains an Analog Signal Processor (ASP) and a Digital Signal Processor (DSP). Implementations of both ASP and DSP are standardized. The key feature of the SCM is the utilization of an inherent ac switching-frequency signal within the power stage. The utilization is in addition to the conventional dc sensing of output voltage v_0, and comparing with a reference E_R. The sensed ac signal and the dc error are processed by the ASP. As a result, total-stage control is obtained. The DSP processes the control-signal output from the ASP in conjunction with a prescribed duty-cycle control law, and operates the on-off of the power switch via a duty-cycle signal d.

In reference [3], a detailed description on the digital signal processor was provided. A standardized implementation scheme for various control, command, and protection blocks was proposed, and actual hardware implementation was performed successfully on the three converter configurations, buck, buck/boost, and the parallel inverters. The following performance improvements were observed and verified in recent modeling and analysis efforts as discussed

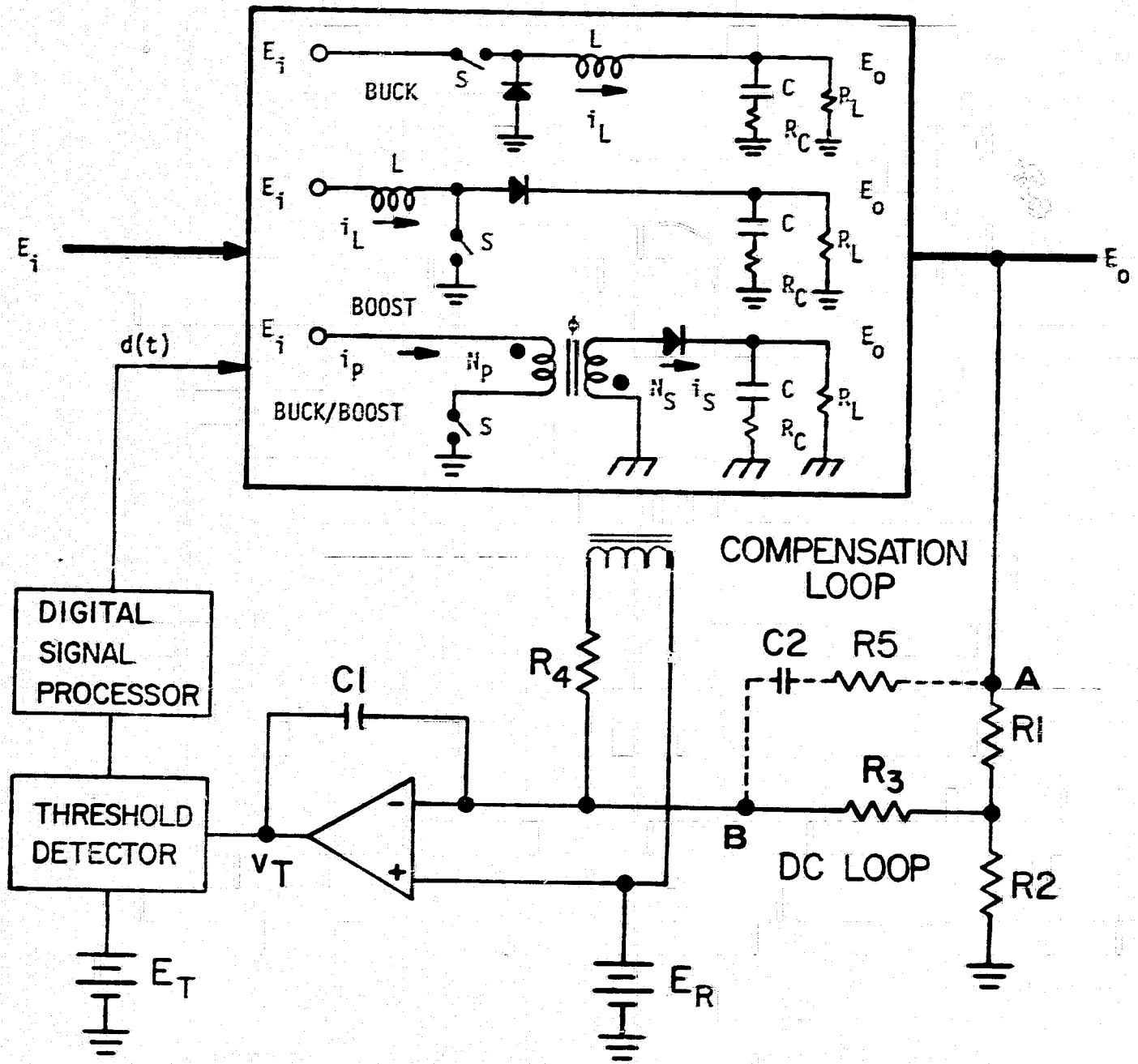


FIG. 1.1. SWITCHING REGULATOR WITH SCM CONTROL

in detail in Volume I of this report, "Application Handbook for a Standardized Control Module for DC-DC Converters."

(1) High-gain, wide-bandwidth, and precision regulation.

(2) Superior dynamic performances, such as audiosusceptibility and transient response.

(3) Stabilization effect by shifting the positive zero on the right-half s-plane to the left-half s-plane.

(4) A control adaptive to the output filter parameter variations due to environmental changes, duty cycle modulations, and capacitive loading.

In the present volume, the SCM User's Design Handbook, the key performance characteristics of SCM-controlled switching regulators derived in Volume I are summarized, and a unified analysis-based design procedure is presented for the three switching regulator types, buck, boost, and buck/boost shown in Fig. 1.1. This procedure enables the designer to select the key SCM control circuit parameters so that for an arbitrarily given power stage, the prescribed performance characteristics concerning stability, audiosusceptibility and transient response can be met concurrently. To accomplish this goal, the universal circuit model shown in Fig. 1.2 is derived for the three SCM regulators. Detailed derivations are presented in Volume I. This common circuit model is employed to examine the following regulator performance categories:

(A) Frequency domain converter performance characteristics:

- Response of v_0 to a sinusoidal disturbance in v_i (audiosusceptibility).
- Response of v_0 to a sinusoidal disturbance in i_0 (output impedance).

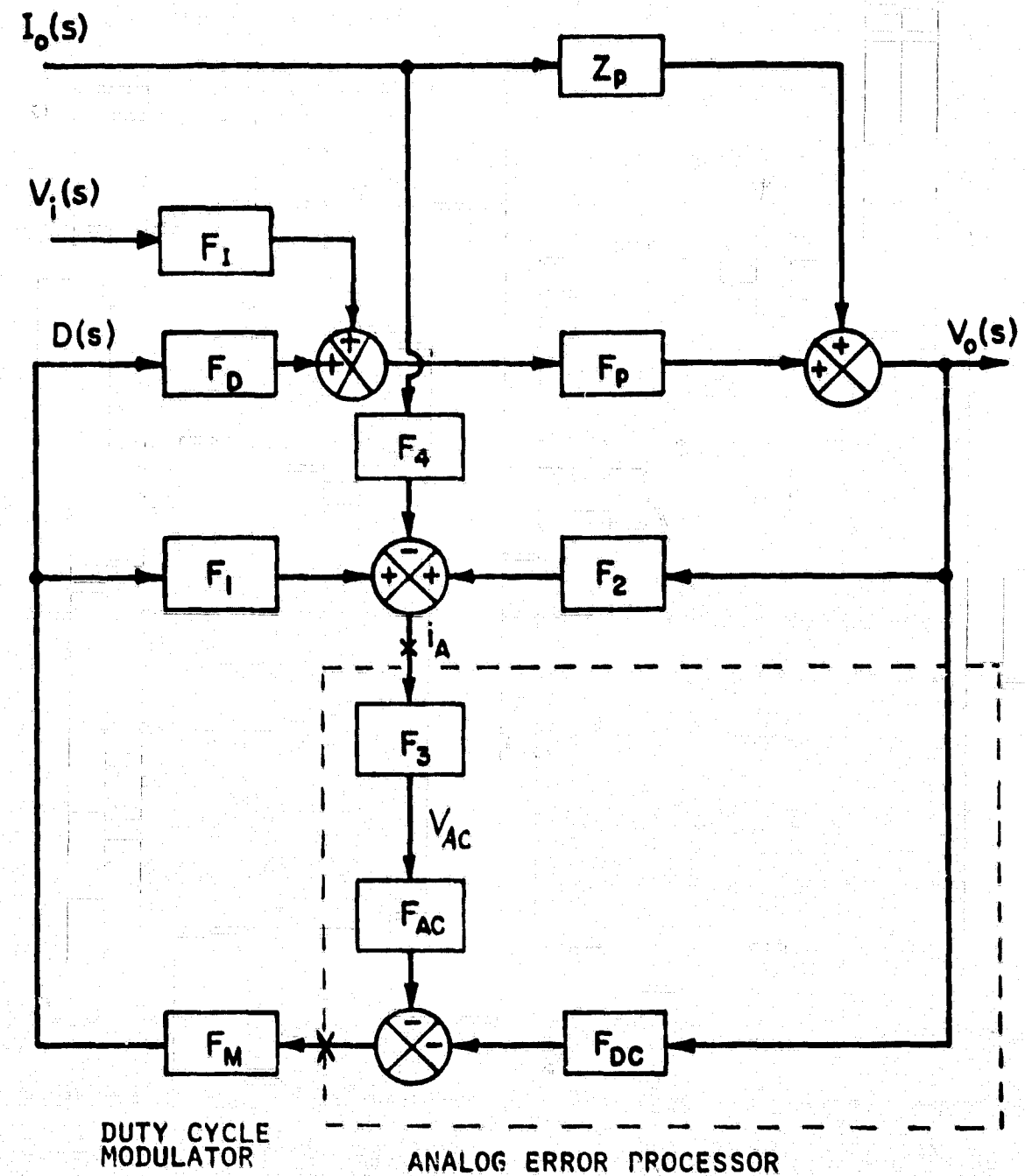


FIG. 1.2 UNIFIED SMALL SIGNAL BLOCK DIAGRAM REPRESENTATION OF FIG. 1.1.

- Response of the regulator loop to a small disturbance in d(t) (stability).

(B) Time domain performance characteristics:

- Response to a step load change.

(C) DC regulation of the converter.

A normalization procedure for the power stage parameters is employed such that the mathematical expression for each performance category has a common form for all three switching regulator types.

Employing the common block diagram representation, the SCM design guidelines for arbitrarily given power stage configurations and element values are represented in analytical form when available, and graphical form when necessary. A simple design procedure is presented such that the regulator performance specifications, such as stability, audiosusceptibility, and transient response can be satisfied simultaneously. This procedure provides simple and straightforward guidelines for selecting the dc loop, ac loop, and RC compensation loop parameters for adaptive compensation to the output filter parameter variations and optimization of the regulator audiosusceptibility and transient response.

The design procedure virtually eliminates the often painful and time consuming iterative paper and bench design process. Several design examples are illustrated with good laboratory support.

CHAPTER 2

DESCRIPTION OF SCM ON BASIC DESIGN CONSIDERATIONS

The objective in Chapter 2 is to inform the user just what SCM is, and why he should apply it in converter design.

2.1 SCM Circuit Descriptions

The standardized control module applied to the three basic switching converters is shown in Fig. 2.1. The SCM consists of two parts: (1) the analog signal processor; and (2) the digital signal processor. The analog signal processor, employing three feedback loops (dc, ac, and compensation loops), processes the error signals to achieve optimal control for various loop-dependent performances such as stability, audiosusceptibility, and transient response. The digital signal processor processes all incoming control signals including error signals from regulator control loops, command and protection and duty cycle timing signals. A brief description for both the analog signal processor and the pulse modulator is provided in the following.

(A) Analog Signal Processor.

Three input signals are applied to the amplifier through three feedback loops working in unison. The dc loop senses the output of the regulator and compares it to the reference voltage E_R to generate a dc error signal e_{dc}. In conjunction with an externally-generated threshold level E_T, the dc output of the amplifier is determined by e_{dc}. This loop is no different than that of any other single-loop error amplifier. The ac loop senses the ac voltage across the energy storage inductor. Since the inductor voltage is of rectangular

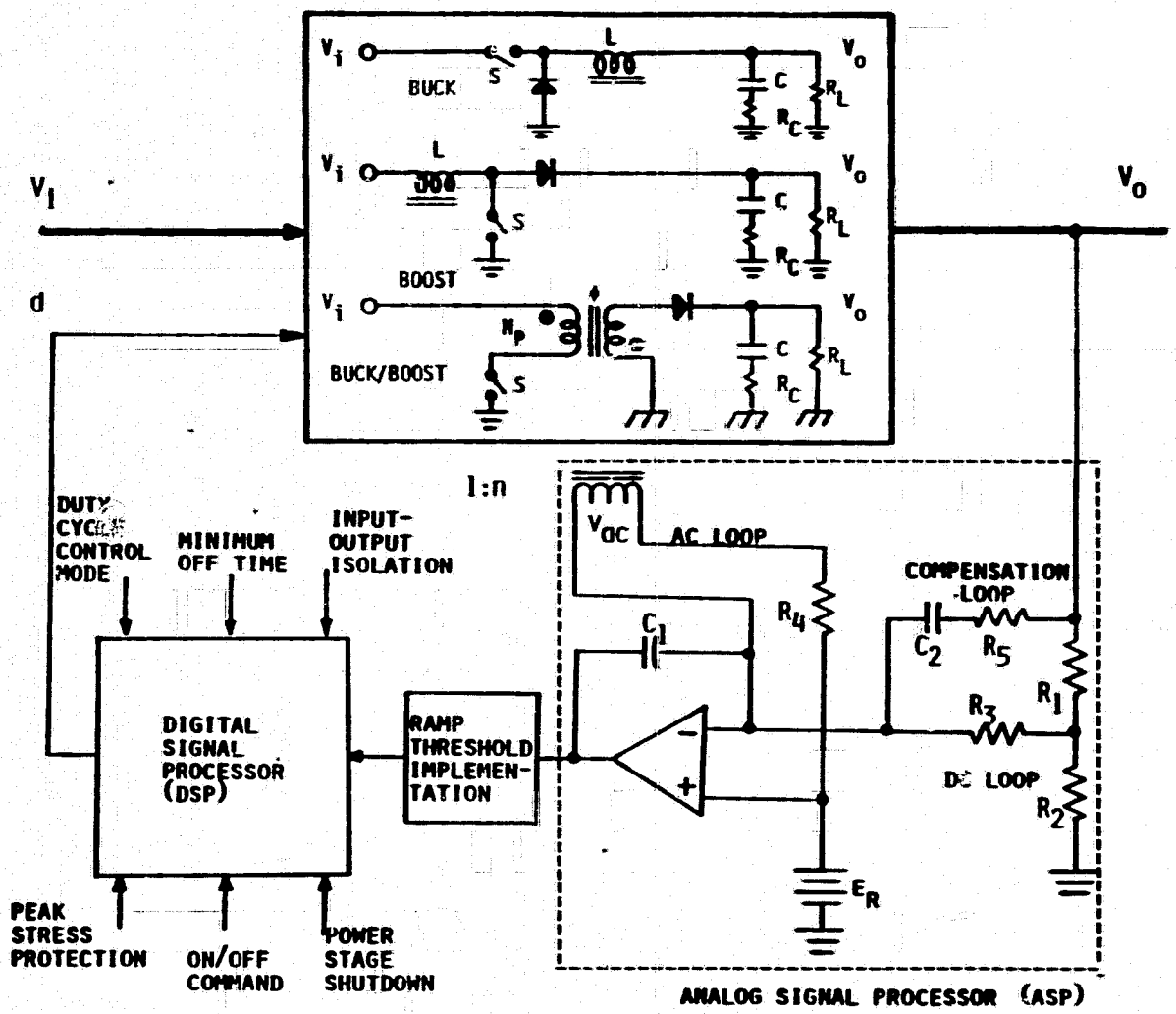


Fig. 2.1 SCM CONTROLLER SWITCHING REGULATORS/BLOCK DIAGRAM

waveform, a triangular ramp is conveniently achieved through the integration of the rectangular voltage. In this case the amplifier is configured with capacitive feedback to serve the dual function of amplification and integration. The third loop, an RC compensation network, senses any change in dv_0/dt, and feeds this information to the integrator amplifier in order to improve regulator performance. The significance of this network is described in detail in Volume I, and in references (4,5,6,7).

(2) Digital Signal Processor.

The digital signal processor (pulse modulator) is the nerve center of the control system, and must process all incoming control signals and transmit the correct output signal to operate the power switch. The signal processed by the digital signal processor encompasses control signals and protection/command signals.

The SCM is capable of operating in several different duty cycle control modes based on different ramp and threshold-level implementations:

1) Pulse frequency modulation.
   - constant T_n, variable T_f
   - constant T_f, variable T_n

2) Pulse with modulation -- constant frequency with variable T_n and variable T_f.

3) Mixed pulse width and pulse frequency modulation -- two-threshold-level control with variable frequency, variable T_n and variable T_f.

The standardized implementation of the digital signal processor including various duty-cycle control, command, and protection signals is discussed in detail in Reference (3).

2.2 Merits of SCM

The electrical performance of a power processor depends, to a large extent, on the quality of its control system. While numerous control circuits have been proposed and are in use today, most of these circuits suffer shortcomings that tend to restrict their utility. The SCM, on the other hand, overcomes many of these shortcomings. Some features of the SCM are:

1) Ability to perform different modes of duty-cycle control.

Various control laws can be used to govern (modulate) the power switch conduction (ON) and nonconduction (OFF) intervals to achieve a given control objective. The available means of timing implementation are: Constant on-time T_n, variable off time T_f; Constant T_f, variable T_n; Constant $(T_n + T_f)$, variable T_n and T_f; Variable T_n, T_f, and $(T_n + T_f)$. While it is quite often true that the means employed to accomplish the control objective is irrelevant as long as all specifications are met, there are certain power processors for which the use of specific means of duty-cycle control is necessary. For example, requirements on synchronization and electromagnetic compatibility may dictate a control based on constant $(T_n + T_f)$, whereas in certain LC resonant applications, the sinusoidal current in the power switch for one half of the LC resonant cycle inherently demands a control based on a constant T_n and a variable T_f. Under special circumstances, one

particular modulation scheme may offer distinct advantages over another from the point of view of protection or transient response.

(2) Ability to provide power-component stress limiting.

One of the most lagging aspects of present power processing technology is reliability. The reliability of the power processors can be greatly enhanced by controlling the power component stresses during steady state, and more significantly, during dynamic operations such as step line and/or load changes, sudden output short circuiting, and converter starting. Without this stress control, the reliability data based on the aggregation of component statistical failure rates becomes meaningless, and no amount of elaborate quality assurance can increase the level of confidence. Thus in the magnetic-semiconductor, transient-prone power processors, the means of achieving reliability enhancement is to implement circuit techniques to instantaneously limit the electrical stresses in all power processor components, thus ensuring safe operation during steady state and transients. Existing power processors often forsake this limiting function, and rely instead on generous derating of all power components to foster reliable operations. Such a practice forces the power processor to remain at the mercy of uncontrolled transient stresses and will inevitably become impractical in future high power applications.

(3) Ability to provide immunity to output-filter parameter changes.

Sources of output-filter parameter changes include initial component tolerances, temperature variations, aging, and most significant, the possible reactive nature of the power-processor load. It is not uncommon for a user's load package to have an input filter with higher capacitance than that of the power-processor output filter. A power processor seldom

enjoys the luxury of having the nature of its loads well defined when it is under development. As a result, the compensation networks of most existing control circuits are devised from consideration of the power-processor output filter alone assuming a resistive load. Exotic means of pole-zero cancellation have been the prevailing art used in negating the second-order filter effect to achieve stability and well-damped responses. Needless to say, such a cancellation can miss its mark badly when tolerance, temperature, aging, and reactive loading have collectively made their presence felt.

(4) Ability to provide adaptive compensation to the moving poles.

The complex poles of the boost and buck/boost converters are affected by the duty cycle of the power switch. The duty-cycle variation which results from line voltage changes is known to produce two moving poles (9,10) which are very difficult to compensate when conventional control means are used. Because of these moving poles, a well compensated regulator, stable under nominal operating conditions, can become unstable under extreme line/load conditions. The SCM control can provide second-order zeros adaptive to the moving poles of the power stage. The stability margins are therefore maintained throughout the entire operating range.

(5) Ability to shift the zero from the right-half s-plane to the left-half s-plane.

It is known that a positive zero (a zero in the right-half s-plane) exists in the power-stage transfer function of the boost and buck/boost converters (9,10). This positive zero is a function of the duty-cycle ratio of the switch, and produces a 90° phase-delay in addition to the

180^{o} phase delay produced by the output filter of the power stage. This additional phase delay, imposed by the "moving" zero, has to be compensated by the control-circuit design for stable operation, particularly when the input voltage is subjected to a wide-range of variation.

(6) Ability to Provide a Unified Design Approach.

Performance characteristics of dc-dc switching regulators are largely dictated by the particular power stage configuration and control scheme chosen. Often in the design practice, once a power stage is chosen and parts designed, subsequent attention is focused on selecting the most suitable control method and frequency stabilization (compensation) network in order to optimize the overall system performances. The lack of a universal control method and a uniform design strategy often necessitates the undertaking of time consuming paper and bench design iterations which frequently result in incompatible and intricate performance characteristics. The SCM is capable of providing a unified design procedure which enables the designer to select the control circuit parameters so that for an arbitrarily given power stage the prescribed performance characteristics concerning stability, audiosusceptibility, and transient response can be met concurrently.

2.3 Design Consideration for SCM Handbook.

In the earlier reports (2,3), detailed description on the digital signal processor was provided. A standardized implementation scheme involving individual building blocks for various control, command, and

protection signals was proposed, and actual hardware implementation was performed successfully for the three converter configurations: buck, buck/boost and the parallel inverters. Attention is now being focused on development of analysis-based design guidelines for selecting control parameters in the ASP in order to achieve the following specified dynamic performances in one non-iterative design attempt:

A) Frequency domain converter performance characteristics.

- Response of v_0 to a sinusoidal disturbance in v_1 (audio-susceptibility).
- Response of v_0 to a sinusoidal disturbance in i_0 (output impedance).
- Response of the regulator loop to a small disturbance in d(t) (stability).

B) Time-domain performance characteristics.

- Response to a step load voltage.

C) DC regulation of the converter.

CHAPTER III
ANALYTICAL MODELS AND PERFORMANCE CHARACTERISTICS

As presented in Volume I of this report, the three basic SCM switching regulators, buck, boost and buck/boost shown in Fig. 1.1, can be represented by the common frequency domain block diagram shown in Fig. 1.2. This diagram incorporates disturbances from the line $\hat{v}_i$, the load $\hat{i}_o$, and the duty cycle control loop $\hat{d}$. This common block diagram representation is employed to evaluate various control-loop dependent regulator performances such as stability, audio-susceptibility and transient response. In order to formulate analysis-based SCM design guidelines to meet a given set of performance specifications, the model is simplified by omitting certain non-essential terms and high-frequency effects. In doing so, a comprehensive design procedure becomes mathematically tractable. A normalization procedure for the converter power stage parameters is used so that the mathematical expression for each performance category enjoys a common form for all three regulator types.

3.1 System Modeling and Block Diagram Representation.

The three basic functional blocks of an SCM-controlled converter are the power stage, the analog-signal-processor (ASP), and the digital signal processor (DSP). Modeling and analysis of these blocks was performed in Volume I. Subsequently, the common frequency domain block diagram shown in Fig. 1.2 was developed. This common block diagram representation is employed in the present report for performance

evaluations, and later, control-circuit design. For convenience of reference, the transfer functions for all blocks shown in Fig. 1.2 are summarized in Table 3.1 for each power stage. Only the continuous inductor current mode is considered in this volume.

A brief description for each block is given in the following.

A. Power stage transfer functions F_1, F_D, F_p, Z_p, F_1, F_2, F_3 and F_4:

The power stage transfer function model incorporates all possible forms of small signal disturbances including the line disturbances $\hat{v}_i$, the load disturbance $\hat{i}_o$, and the duty cycle disturbance $\hat{d}$. This model provides both dc and ac error signals to the analog signal processor.

The power stage transfer functions are defined as follows:

$F_p(s)$: Equivalent output filter transfer function.

$F_I(s)$: Input voltage gain, ($F_I F_p$ represents the open loop input-to-output-voltage transfer function).

$F_D(s)$: Duty cycle gain, ($F_D F_p$ represents the duty-cycle-to-output-voltage gain).

$F_p(s)$: The output impedance of the open-loop converter power stage, ($Z_p \hat{i}_o$ represents the open-loop output voltage variation due to the load current disturbance $\hat{i}_o$).

The next two transfer functions are employed to provide the ac error signal (the voltage across the ac loop sensing winding voltage $\hat{v}_{ac}$ shown in Fig. 1.1):

$F_1(s)$ and $F_2(s)$: Together, these functions provide the small-signal low-frequency ac inductor current (or magnetic flux) due to disturbances from the output voltage $\hat{v}_o$ and duty cycle $\hat{d}$.

It should be noted that the feed-forward path through F_1 exists for the boost and buck/boost converters because the inductor for these two configurations is separated from the output filter capacitor by a switch. As a result the equivalent inductance in the small-signal model is modulated by the duty cycle of the switch.

$F_3(s)$: Impedance function employed to convert the inductor current or magnetic flux into an ac error voltage $\hat{v}_{ac}(s)$ across the sensing winding.

$F_4(s)$: Transfer function characterizing the amount of disturbance of the inductor current due to load disturbance.

B. Analog signal processor (ASP) transfer functions: F_{DC} AND F_{AC}:

The analog signal processor combines the dc error signal $\hat{v}_o$ and the ac error signal $\hat{v}_{ac}$ to form a total state control. The output of ASP is fed to the input of the duty cycle pulse modulator.

$F_{DC}(s)$: The transfer function of the combined dc loop and RC compensation loop.

$F_{AC}(s)$: The transfer function of the ac loop.

C. Duty cycle pulse modulator transfer function F_M.

F_M: The describing function of the duty cycle pulse modulator. Table 3.2 presents the duty-cycle describing function models for constant T_{on} control, constant T_{off} control, and constant frequency control with and without an external ramp. As discussed in Volume I and references (3,4,5,8), the constant frequency control is inherently unstable when the duty cycle is greater than 50 percent with the constant-frequency clock initiating the turn-on time and less than 50 percent with

Table 3-I Summary of Transfer Functions for All Functional Blocks.

Block \ Power Stage	Buck	Boost	Buck-Boost
F_I	D	$\frac{1}{D'}$	$\frac{D}{D'}\ \frac{N_S}{N_P}$
F_D	$\frac{V_0}{D}$	$\frac{V_0}{D'}\left(1-s\frac{L_e}{R_L}\right)$	$\frac{V_0}{DD'}\left(1-\frac{sDL_e}{R_L}\right)$
F_1	0	$\frac{V_0}{(D')^2R_L}$	$\frac{V_0}{(D')^2R_L}$
F_2	$\frac{1+sCR_L}{R_L(1+sCR_C)}$	$\frac{1}{D'R_L}\frac{1+sCR_L}{1+sCR_C}$	$\frac{1}{D'R_L}\frac{1+sCR_L}{1+sCR_C}$
F_3	snL	snL	snL_S
F_4	1	$\frac{1}{D'}$	$\frac{1}{D'}$
F_P	$\frac{1+sCR_C}{\Delta}$		$\Delta = s^2+s\left(\frac{1}{CR_L}+\frac{R_{eq}+R_C}{L_e}\right)+\frac{1}{L_eC}$
Z_P	$F_P\cdot(R_{eq}+sL_e)$		
F_{AC}	$\frac{1}{sC_1R_4}$		
F_{DC}	$\frac{1}{sC_1}\left(\frac{g}{R_3+R_x}+\frac{1}{Z_C}\right)$,		$R_x = R_1 /\!/ R_2, g = \frac{R_x}{R_1}, Z_C = R_5+\frac{1}{sC_2}$
F_M	$2R_4C_1/(nM)$		see Table 7-I for M

TABLE 3.2 PULSE MODULATOR GAIN $F_M = \frac{2R_4C_1}{N}\frac{1}{M}$

(CONTINUOUS CURRENT OPERATION)

M	CONSTANT T_{ON}	CONSTANT T_{OFF}	CONSTANT T W/O RAMP	CONSTANT T WITH RAMP
BUCK	$V_I T_{ON}$	$V_I T_{OFF}$	$V_I(1-2D)T$	$V_I(1-2D)T + 2sT\frac{R_4C_1}{N}$
BOOST	$V_0 T_{ON}$	$V_0 T_{OFF}$	$V_I(2-\frac{1}{D'})T$	$V_I(2-\frac{1}{D'})T + 2sT\frac{R_4C_1}{N}$
BUCK/ BOOST	$(\frac{N_S}{N_P}V_I + V_0)T_{ON}$	$(\frac{N_S}{N_P}V_I + V_0)T_{OFF}$	$\frac{N_S}{N_P}V_I(1-\frac{D}{D'})T$	$\frac{N_S}{N_P}V_I(1-\frac{D}{D'})T + 2sT\frac{R_4C_1}{N}$

the clock initiating the turn-off time. The constant frequency F_M given in Table 3.2 corresponds to the former case when the clock initiates the turn-on time. When the duty cycle is greater than 50 percent, M becomes negative. The negative F_M together with a negative feedback thus forms an unstable positive feedback system.

3.2 Normalization

To facilitate analysis and design for the three converter types, a normalization procedure for the power stage parameters is proposed. The mathematical expression for each performance category of the normalized system enjoys a common form for all three switching regulator types.

$$\text{Let } s(\text{normalized}) = \frac{1}{\omega_o} s'(\text{unnormalized}) \tag{3.1}$$

Then,

$$F_p(s) = \frac{\tau_{z1}\omega_o s + 1}{s^2 + 2\zeta s + 1} \frac{1}{\omega_o^2} \tag{3.2}$$

$$\text{where } \omega_o = \frac{1}{\sqrt{L_e C}} \tag{3.3}$$

$$\zeta = \frac{\omega_o}{2}\left[\frac{L_e}{R_L} + (R_{eq} + R_C)C\right] \tag{3.4}$$

$$\tau_{z1} = R_c C \tag{3.5}$$

$$L_e = \begin{cases} L & \text{buck} \\ L/D'^2 & \text{boost and buck/boost} \\ L_s/D'^2 & \text{buck/boost} \end{cases} \tag{3.6}$$

$$R_{eq} = \begin{cases} R_\ell & \text{buck} \\ \dfrac{R_\ell}{D'^2} + \dfrac{D}{D'}\, R_c & \text{boost} \\ \dfrac{R_s}{D'^2} + \dfrac{D}{D'}\, R_c & \text{buck/boost} \end{cases} \tag{3.7}$$

where $D \triangleq T_{on}/T_p$, $D' \triangleq T_{off}/T_p$ and R_ℓ is the winding resistance of the inductor. For the two-winding buck/boost converter, R_s represents the winding resistance of the secondary winding.

In addition, the following expressions are used in the disucssion which follows:

$$\tau_{p1} = R_5 C_2 \tag{3.8}$$

$$\tau_{z2} = (R_5 + R_y)C_2 \tag{3.9}$$

$$F_M = \frac{2R_4 C_1}{nM} \tag{3.10}$$

where n is the turn ratio between the sensing winding and the inductor winding, and $R_y = (R_3 + R_1 \parallel R_2)\, R_1/(R_1 \parallel R_2)$. (3.11)

3.3 Stability Analysis

The classical Bode analysis technique is employed to investigate the open-loop gain and phase. For a multiple-loop control system, the "loop-opening" should be performed at a place common to all feedback paths. It is clear from Figure 1.2 that such a place is the path containing the block F_M. By opening the loop at the point marked X, the open-loop transfer function based on the various blocks of Figure 1.2 is obtained. Using the open-loop transfer function, the detailed transfer function can be expressed in terms of circuit parameters. Prior to simplification, the detailed equations reveal how the various SCM parameters should be designed to achieve ample stability margin. The SCM feature of adaptive stability is then made apparent.

The open-loop transfer function can be expressed as

$$G_T(s) = F_M[F_{AC}F_1F_3 + F_PF_D(F_{DC} + F_3F_2F_{AC})] \qquad (3.12)$$

The transfer function is applicable to all three power stages. Substituting contents of Table 3.1 into (3.12), and assuming $\tau_{p1} = \tau_{z1}$ (see section 4.3 for detailed discussion) the open-loop transfer functions $G_T(s)$ of the normalized system can be derived as

$$G_T(s) = \frac{K_1}{\omega_o s} \frac{A_1\alpha'}{1+A_2\alpha'\tau_{z2}} \frac{\frac{1}{\alpha'}s^2+\tau'_{z2}\omega_o s+1}{s^2+2\zeta s+1}$$

$$= \frac{K_1\alpha}{\omega_o s} \frac{\frac{1}{\alpha'}s^2+\tau'_{z2}\omega_o s+1}{s^2+2\zeta s+1} \quad . \tag{3.13}$$

where the parameters K_1, ω_o, α, α', τ'_{z2} and ζ are assigned different values for different converter configurations. The parameters α and α' are defined by the equations:

$$\left.\begin{aligned} \alpha &= \frac{R_4}{nR_y} && \text{buck} \\ &= \frac{R_4}{nR_yD'} && \text{boost and buck/boost} \end{aligned}\right\} \tag{3.14}$$

and

$$\alpha' = \frac{\alpha}{A_1 - A_2\tau_{z2}\alpha} \quad \text{or} \quad \alpha = \frac{A_1\alpha'}{1+A_2\alpha'\tau_{z2}} \tag{3.15}$$

For most practical designs, $\alpha' \simeq \alpha$. The other parameters are defined by the equations:

$$\left.\begin{aligned} A_1 &= 1 && \text{buck} \\ &= 1 - \frac{R_{eq}}{R_L} + \frac{2\zeta\omega_o L_e}{R_L} - \left(\frac{L_e\omega_o}{R_L}\right)^2 && \text{boost} \\ &= 1 - \frac{DR_{eq}}{R_L} + \frac{2\zeta\omega_o DL_e}{R_L} - D\left(\frac{L_e\omega_o}{R_L}\right)^2 && \text{buck/boost} \end{aligned}\right\} \tag{3.16}$$

$$A_2 = 0 \quad \text{buck}$$
$$= 1/(R_L C) \quad \text{boost}$$
$$= D/(R_L C) \quad \text{buck/boost} \qquad (3.17)$$

$$\tau'_{z2} = \tau_{z2} \quad \text{buck}$$
$$= [\tau_{z2} + \frac{L_e}{\alpha R_L}](1 - \frac{R_{eq}}{R_L}) + \frac{L_e}{\alpha R_L}(1 - \alpha) \simeq \tau_{z2} \quad \text{boost}$$
$$= [\tau_{z2} + \frac{L_e}{\alpha R_L}](1 - \frac{DR_{eq}}{R_L}) + (1 - \alpha)\frac{DL_e}{\alpha R_L} \simeq \tau_{z2} \quad \text{buck/boost} \qquad (3.18)$$

$$K_1 = \frac{2V_I}{M} \quad \text{buck}$$
$$= \frac{2V_I}{D'M} \quad \text{boost}$$
$$= \frac{Ns}{N_p}\frac{2V_I}{DM} \quad \text{buck/boost} \qquad (3.19)$$

It is important to note that the open loop characteristics of the three different converter circuits using SCM control are converted into the same form. This finding has significant impact on the basic design philosophy. It is commonly known that the small signal characteristic of the boost and buck/boost converters, unlike the buck converter, has a positive zero which introduces addition phase delay. Employing a conventional single-loop control, an additional compensation scheme is needed to stabilize the converter. Nevertheless.

when SCM is employed the positive zero of the boost or buck/boost converter is shifted to the left-half s-plane such that the open loop characteristics for all three converters share a common form. In addition a second-order zero is generated by SCM control to compensate the second-order pole of the output filter. The SCM has thus mitigated to a large extent the particular instability concerns of boost and buck/boost regulators. (For detailed discussions, please refer to chapter 9 of Volume I.)

The two zeros of eq. (3.13) can be expressed as:

$$s_{o1}, s_{o2} = \frac{\alpha' \omega_o \tau'_{z2}}{2}\left[1 \pm \sqrt{1 - \frac{4\alpha'}{(\alpha' \omega_o \tau'_{z2})^2}}\right] \tag{3.20}$$

The open loop transfer function is expressed as

$$G_{T(s)} = \frac{\alpha K_1}{\omega_o s} \frac{(s/s_{o1}+1)\ (s/s_{o2}+1)}{s^2 + 2\zeta s + 1} \tag{3.21}$$

The locus of the second-order zero of (3.20) is illustrated in Fig. 3.1 for a fixed $\alpha' = 1$ and variable τ'_{z2}. As the magnitude of τ'_{z2} increases the second-order zero changes from a complex-conjugate pair to two negative real zeros. It is interesting to note that a complete pole-zero cancellation can be achieved for the case of $\alpha' = 1$ and $\omega_o \tau'_{z2} = 2\zeta$. Since s_{o1} and s_{o2} are also functions of ω_o, the pole-zero cancellation is held true for any arbitrary filter L and C values. A control adaptive to filter parameter changes is thus realized. However, as discussed in detail in Volume I, in order to achieve higher loop gain and wider bandwidth for performance optimization it is desirable to have two negative real zeros instead of complex conjugated zeros. For negative real zeros, the following inequality should be satisfied:

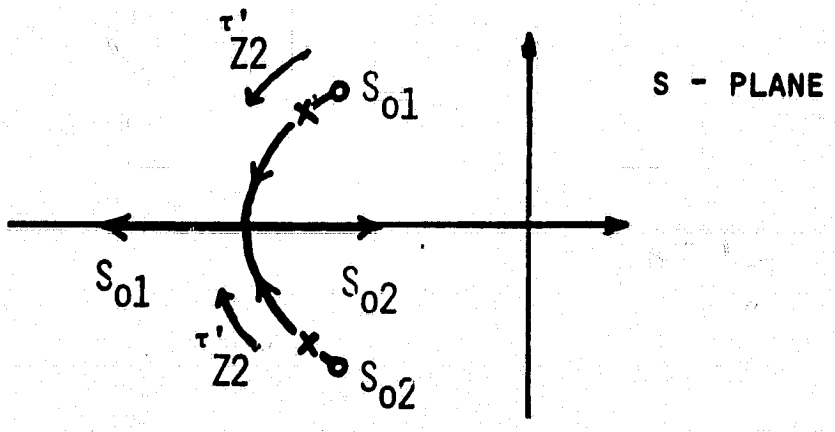


FIG. 3.1 POLES AND ZEROS OF THE OPEN LOOP TRANSFER FUNCTION

$$\frac{4}{\alpha'(\omega_o \tau'_{z2})^2} < 1 \qquad (3.22)$$

Then the following simplified expression can be obtained

$$s_{o1} \approx \alpha' \omega_o \tau'_{z2} \qquad (3.23)$$

$$s_{o2} \approx \frac{1}{\omega_o \tau'_{z2}}$$

The above assumption is valid if the two zeros s_{o1} and s_{o2} are sufficiently apart. This inequality is not only desirable in order to simplify the design procedure, it also improves the dynamic performance of switching regulators as discussed in detail in Volume I.

The qualitative behavior of the open loop characteristic is examined based on the simplified equations (3.23).
Consider an arbitrary case where the asymptotic curves of (3.21) are shown in Figure 3.2. If all corner frequencies are sufficiently apart, the following approximations hold true.

$$\begin{aligned}
&s < s_{o2} && G_T(s) \approx \frac{\alpha K_1}{\omega_o s} \\
&s_{o2} < s < 1 && G_T(s) \approx \frac{-\alpha K_1}{\omega_o s_{o2}} = \frac{-\alpha}{\alpha'} \frac{K_1}{\omega_o} s_{o1} \\
&1 < s < s_{o1} && G_T(s) \approx \frac{-\alpha K_1}{\omega_o s_{o2}} \frac{1}{s^2 + 2\zeta s + 1} \\
&s > s_{o1} && G_T(s) \approx \frac{K_1}{\omega_o s} \frac{\alpha}{\alpha'}
\end{aligned} \qquad (3.23)$$

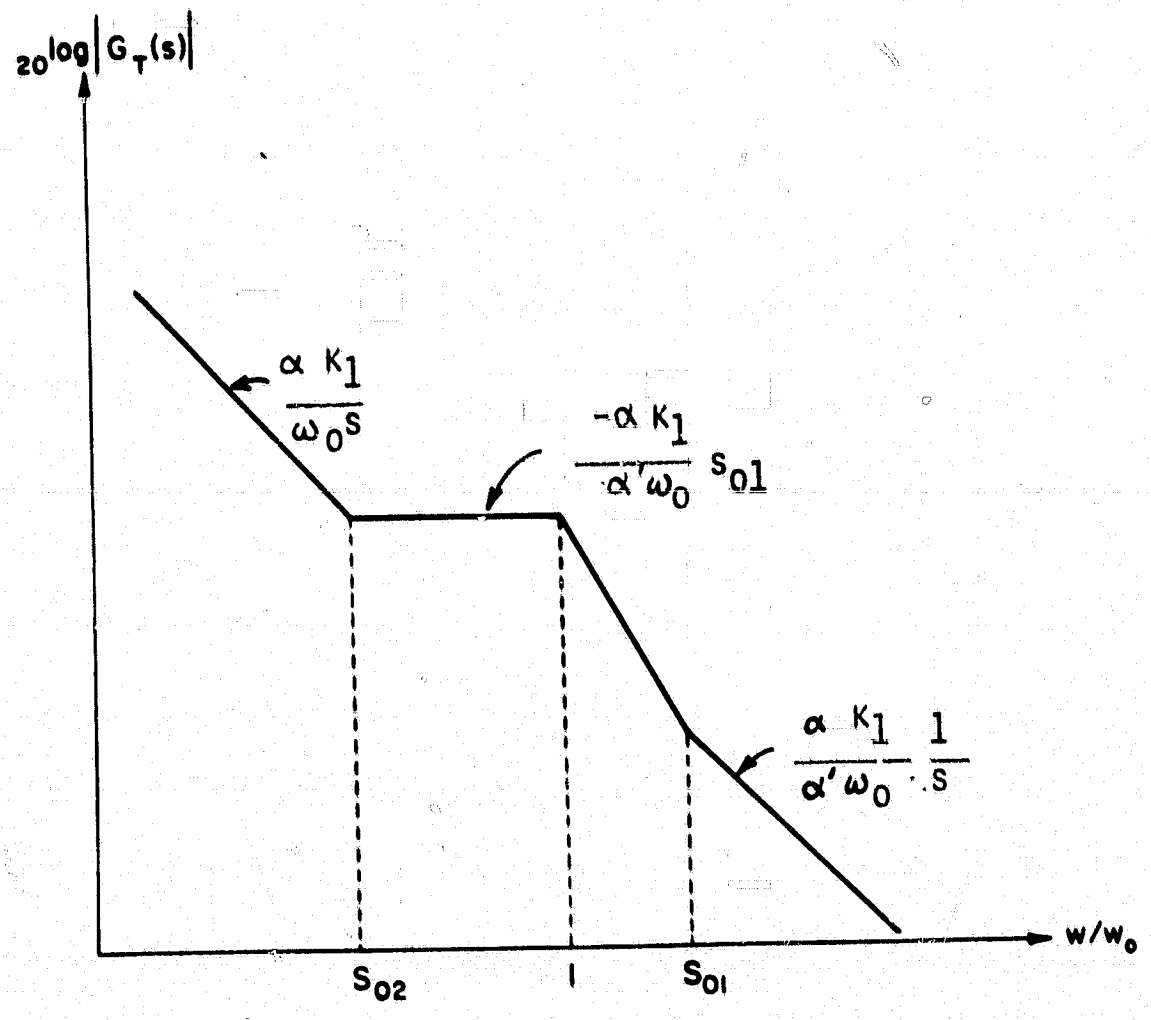


FIG. 3.2 ASYMPTOTIC CURVE OF THE OPEN LOOP TRANSFER FUNCTION

Since K_1 is usually a large number, the open-loop cross-over frequency normally occurs at a frequency above S_{o1} and the open-loop transfer function in the neighborhood of the cross-over frequency can be simply represented by $G_T(s) = \frac{K_1}{\omega_o s} \frac{s}{\alpha'}$. This is a very interesting discovery, since for frequency above S_{o1} the open-loop transfer function is not affected by any control loop parameters.

Proper arrangement of the zeros S_{o1} and S_{o2}, by careful selection of the control parameter values, can result in any desired open-loop characteristic. Figures 3.3(A) and (B) illustrate the effect on gain and phase of changing the location of the zero S_{o1} by varying α'. The zero S_{o2} is kept fixed. Families of gain and phase curves with $\omega_o T'_{z2} = 5.0$ are shown for twelve different values of α'. These values are: 0.04, 0.1, 0.2, 0.4, 0.6, 0.8, 1, 2, 3, 4, 5, and 6. The effect of increasing the value of S_{o1} is to increase the gain at frequencies lower than S_{o1} while keeping the gain constant for frequencies higher than S_{o1}.

In the gain plot of Figure 3.3(a), a higher α' produces a higher gain. However, such a gain is accompanied in the phase plot of Figure 3.3(b) by a correspondingly higher phase angle, resulting in a smaller phase margin. The effect of the parameter α' on the open-loop gain and phase is vividly displayed in the three-dimensional plots Fig.3.4(a) and (b). The family of curves shown in Fig. 3.3 is represented by a three-dimensional surface by introducing a third axis representing the variable α'.

In the above example, a two-winding buck/boost converter with the following parameter values is employed:

L_S = 220 μH, C = 700 μF, R_{eq} = 0.5 Ω, R_C = 0.05 Ω,
R_L = 28 Ω, $N_S = N_P$ = 33 turns, n = 0.667, V_I = 20V,
V_o = 28 V, $\omega_o \tau'_{z2}$ = 5, $M = V_I T_{on}$ = 0.5 x 10^{-3} V-sec.,
τ_{p1} = 0.16 x 10^{-4} sec. and ζ = 0.2

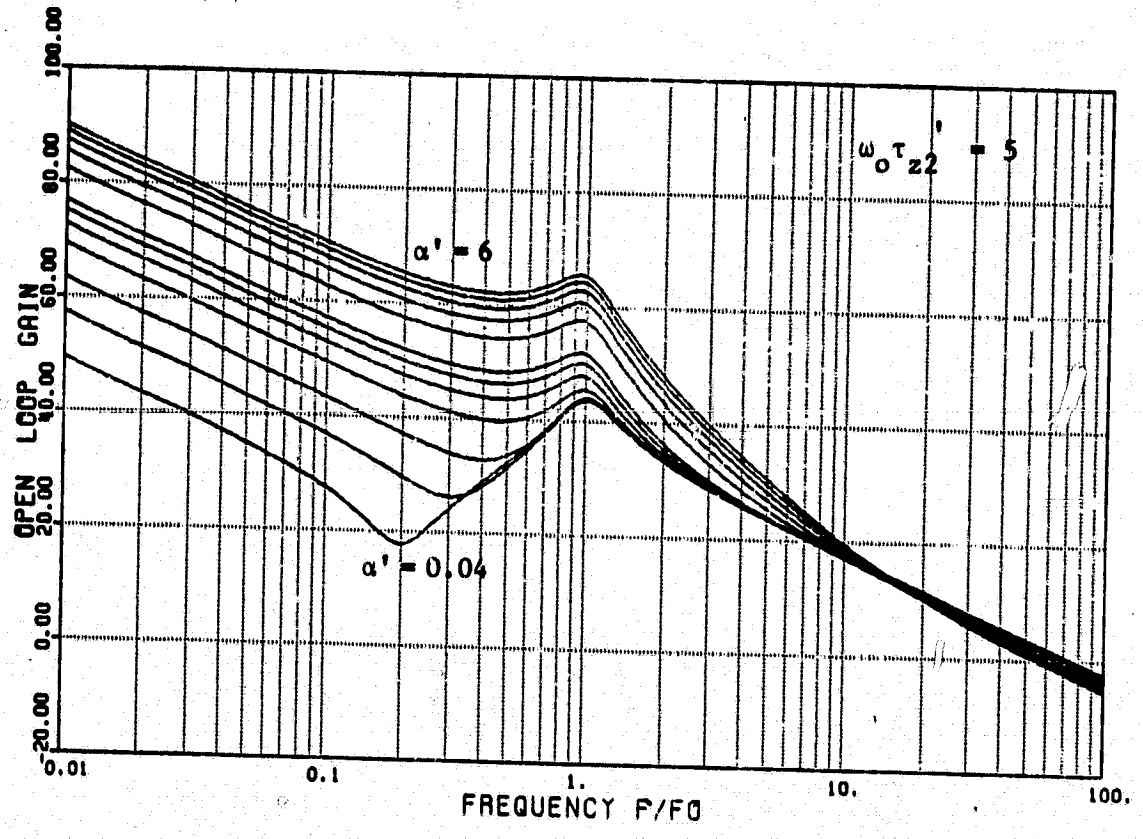


FIG. 3.3(A) OPEN LOOP GAIN CHARACTERISTIC FOR DIFFERENT VALUES OF THE PARAMETER α'; α' = 0.04, 0.1, 0.2, 0.4, 0.6, 0.8, 1, 2, 3, 4, 5, 6 FROM THE BOTTOM CURVE UP, RESPECTIVELY

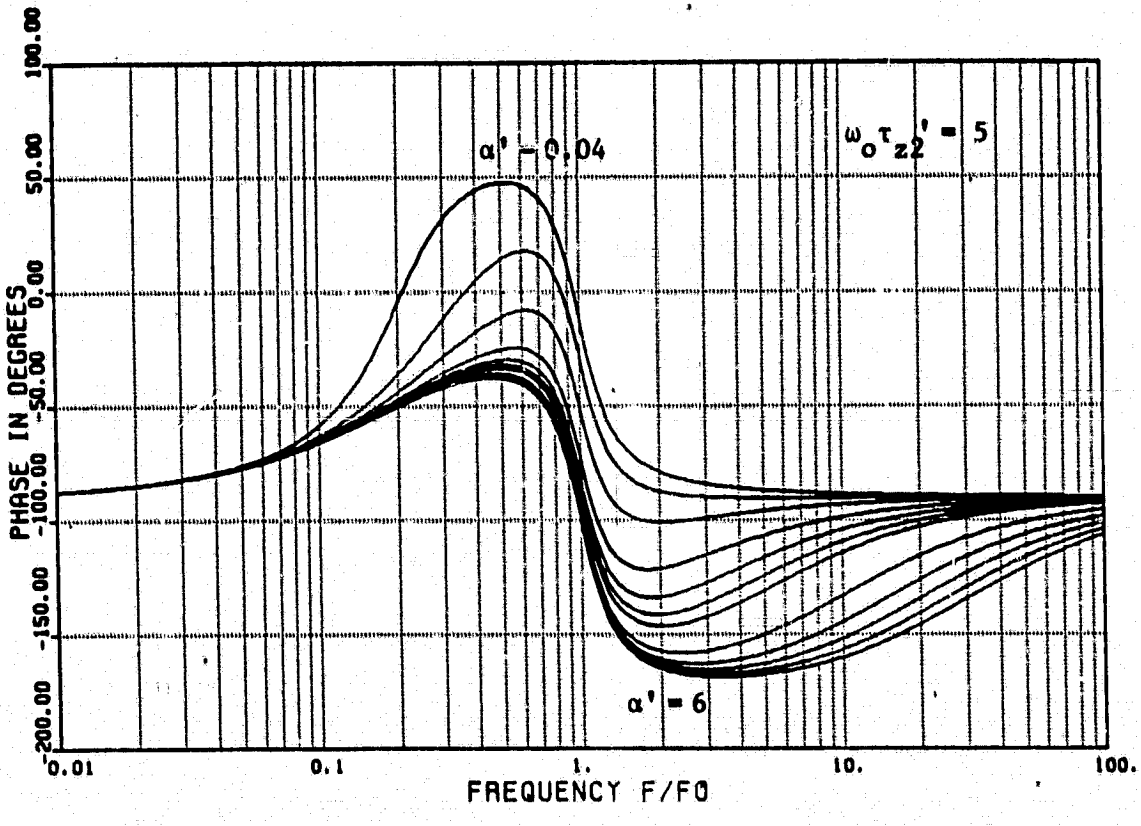


FIG. 3.3(B) OPEN LOOP PHASE CHARACTERISTIC FOR DIFFERENT VALUES OF THE PARAMETER α'; α' = 0.04, 0.1, 0.2, 0.4, 0.0, 0.8, 1, 2, 3, 4, 5, 6 FROM THE TOP CURVE DOWN, RESPECTIVELY

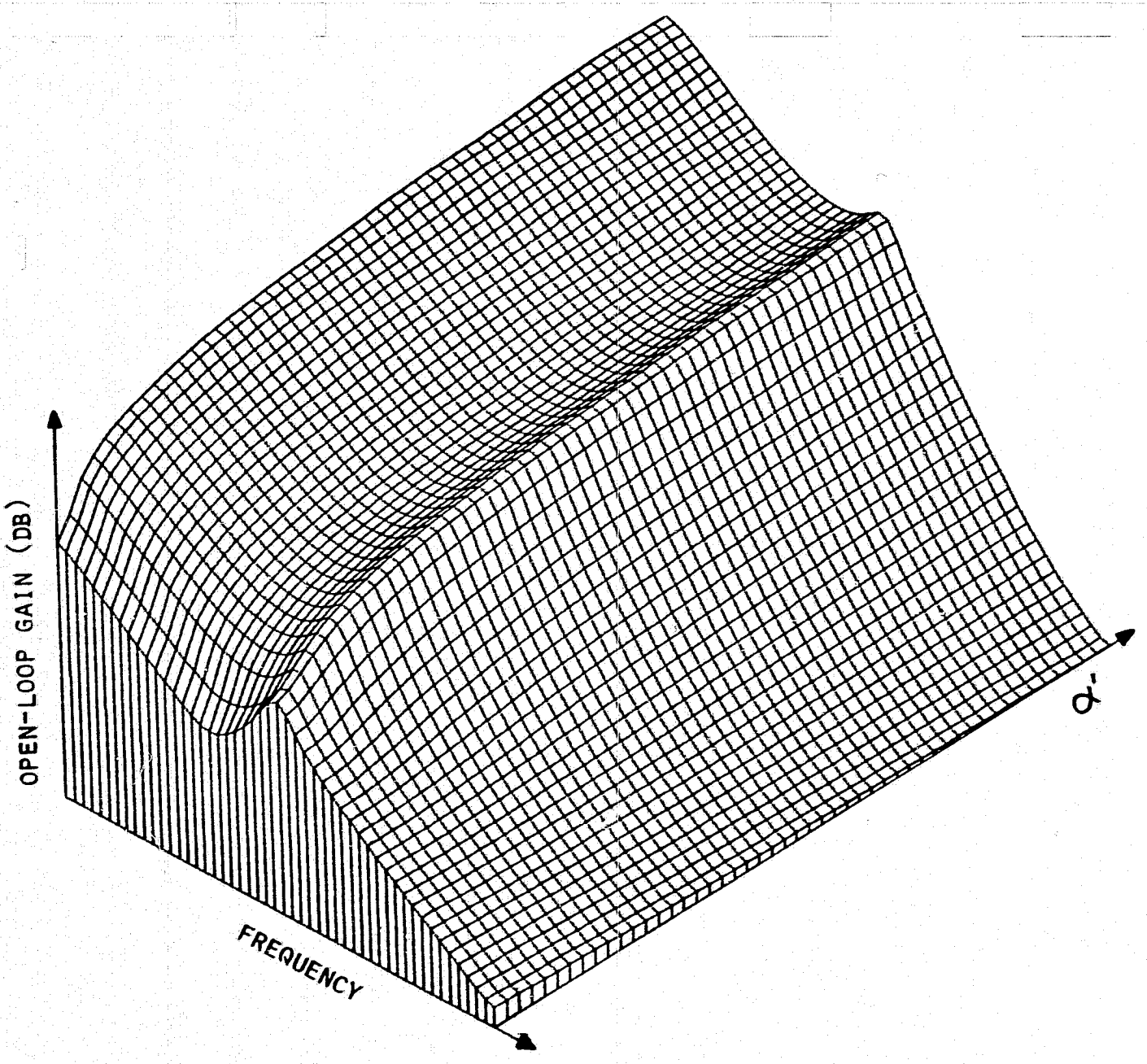


FIG. 3.4(A) THREE-DIMENSIONAL PLOT OF THE OPEN LOOP GAIN SHOWN IN FIG. 3.3(A)

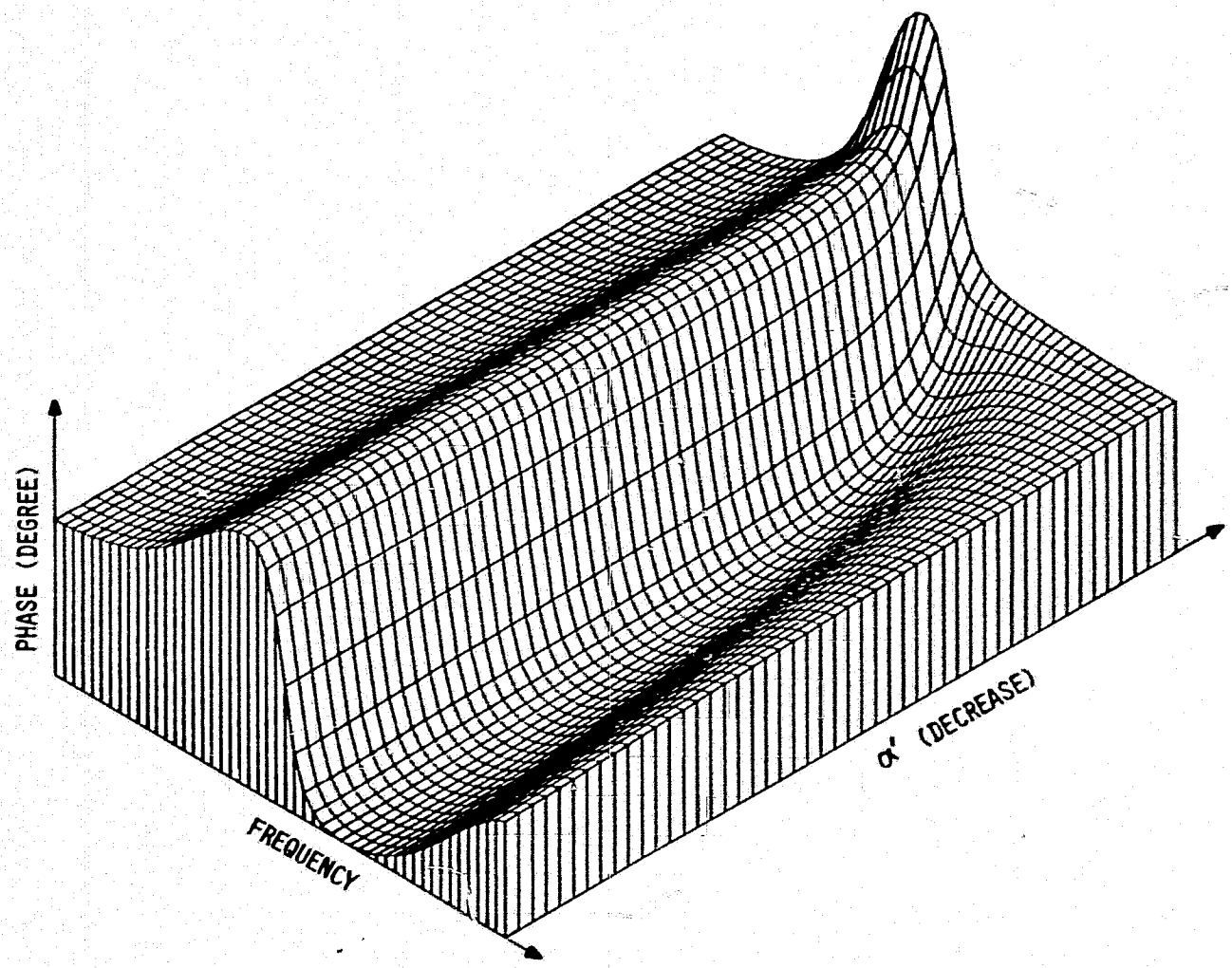


FIG. 3.4(B) THREE-DIMENSIONAL PLOT OF THE OPEN-LOOP PHASE OF FIG. 3.3(B)

3.4 Audiosusceptibility Analysis

Audiosusceptibility refers to the regulator's ability to attenuate a small-signal sinusoidal disturbance propagating from the regulator input to its output. The audiosusceptibility performance is of considerable importance, as the regulators generally share the input bus with other online equipment. The steady-state and dynamic operations of this equipment generate noise voltages on the input line which must be attenuated by the closed-loop regulator so that payload operations at the regulator outputs will not be detrimentally compromised. Since the passive filters in the regulator generally can provide adequate attenuation of disturbances at higher frequencies, interest in audiosusceptbility from a feedback-control-performance viewpoint is more often confined to a lower frequency range within, say, zero to ten times the output filter resonant frequency of the regulator.

The audiosusceptibility analysis utilizes the same block diagram of Figure 1.2 previously used for the stability analysis. Interest is focussed on the voltage ratio $\hat{v}_o/\hat{v}_i$, with output-current disturbance $\hat{i}_o$ assumed to be zero. It is clear that the $\hat{v}_i$ to $\hat{v}_o$ propagation actually portrays the closed-loop frequency response of the regulator.

It is easily proved form Figure 1.2 that the closed-loop frequency response $G_A(s)$ can be expressed as:

$$\frac{\hat{v}_o}{\hat{v}_i} = G_A(s) = \frac{F_I F_p \ (1 + F_1 F_3 \ F_{AC} F_M)}{1 + G_T(s)} \qquad (3.25)$$

where F_I, F_p, F_1, F_3, F_{AC}, and F_M have been defined in Table 3.1. and $G_T(s)$ is the open-loop frequency response derived previously in eq.(3.13).

Substituting the defined parameters in Table 3.1 into (3.25) and applying the normalization of eq. (3.1), one has

$$G_A(s) = \frac{K_2}{1 + G_T(s)} \cdot \frac{\tau_{z1}\omega_o s + 1}{s^2 + 2\zeta s + 1} \tag{3.26}$$

Substituting (3.13) into (3.26), one obtains

$$G_A(s) = \frac{K_2}{K_1}\frac{\omega_o}{\alpha} \cdot \frac{s(\tau_{z1}\omega_o s + 1)}{\frac{\omega_o}{\alpha K_1} s^3 + (\frac{1}{\alpha'} + \frac{\omega_o}{\alpha K_1})s^2 + (\tau'_{z2}\omega_o + \frac{\omega_o}{\alpha K_1})s + (1 + \frac{\omega_o}{\alpha K_1})} \tag{3.27}$$

The closed loop transfer function $G_A(s)$ has two zeros and three poles. For sufficiently large K_1, the three poles are generally negative real and sufficiently apart. However, by increasing the control parameters α' for large loop gain and wider bandwidth as illustrated in Fig. 3.3, the root-locus follows the pattern shown in Fig. 3.5. Notice in Fig. 3.5 that the symbols used for zeros in $G_T(s)$ are now used for the poles in $G_A(s)$, namely s_{o1} and s_{o2}. This is true because the poles of the closed-loop transfer function $G_A(s)$ and the zeros of the open-loop transfer function $G_T(s)$ are approximately the same. In the closed-loop transfer function $G_A(s)$, an additional high-frequency pole is introduced and is represented by s_{o3}. For small α', the roots s_{o1} and s_{o2} form a complex pair. As α' increases, s_{o1} and s_{o2} moves toward the real axis where they merge, then move apart. As α' increases still more, s_{o1} crosses the high frequency zero, then merges with s_{o3} to form another complex pair. The complex roots can result in severe peaking of the audiosusceptibility characteristic. For sufficiently small α' the detrimental peaking of $G_A(s)$ characteristic occurs at low frequency as discussed in detail in Chapter 9 of the companion report. For sufficiently large α', the peaking

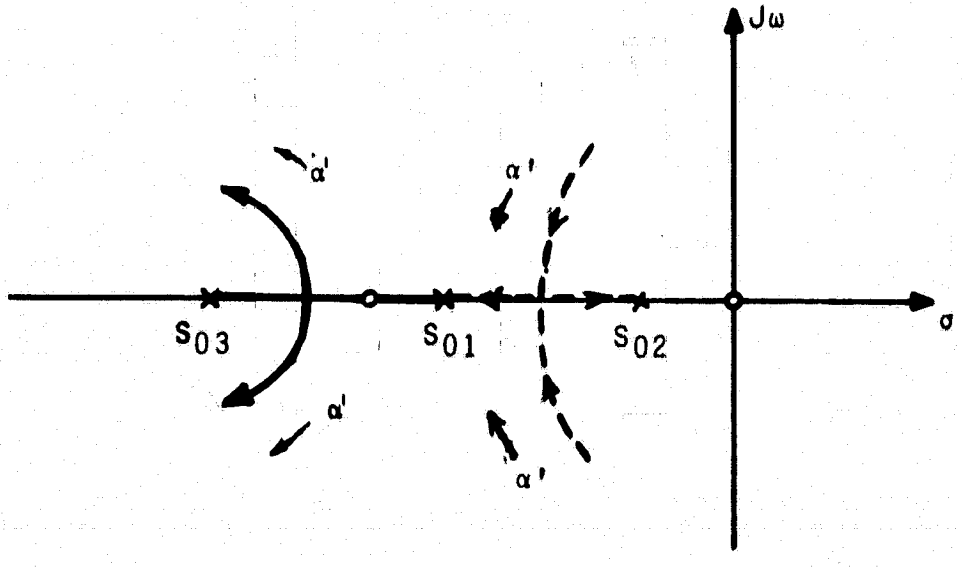


FIG. 3.5 LOCUS OF THE CHARACTERISTIC ROOTS OF $G_A(s)$ AS A FUNCTION OF α'

of $G_A(s)$ characteristic occurs at high frequecies. These peaking phenomena are illustrated in Fig. 3.6 employing a buck/boost converter with the same values as used in Fig. 3.3. The characteristic of $G_A(s)$ as a function of frequency and the control parameter α' can be vividly displayed as the three dimensional surface contour shown in Fig. 3.7.

It is shown that an apparent peaking effect is present at high frequencies for large α'. Such a peaking effect can cause severe degradation of the regulator performance. The effect of high frequency peaking of $G_A(s)$ can be mitigated when an input filter is employed. In contrast to $G_A(s)$, the undesirable high frequency peaking effect in the output impedance characteristic (to be discussed in the next section) cannot be alleviated by an input filter. This high frequency peaking is frequently observed in the laboratory for high-gain, wide-bandwidth regulator design, and the cause is comprehended only now through the analysis effort.

It is important to note that while higher loop gain and wider bandwidth can always be achieved by increasing the α' parameter values as shown in Fig. 3.3, optimum audiosusceptibility performance can only be achieved by judicious selection of α'. Guidelines for selection of control parameters to optimize the audiosusceptibility characteristic may be derived as follows:

The asymptotic curve of $G_A(s)$ for different values of s_{ol} is illustrated in Fig. 3.8. Qualitatively speaking, if s_{ol} is sufficiently small, the worst audiosusceptibility occurs in the low frequency range, while if s_{ol} is sufficiently large, the worst $G_A(s)$ occurs in higher frequency range with possible peaking effect. The following two cases are considered:

$$s_{ol} < 1/(\omega_o \tau_{z1}) \text{ and } S_{ol} > 1/(\omega_o \tau_{z1}).$$

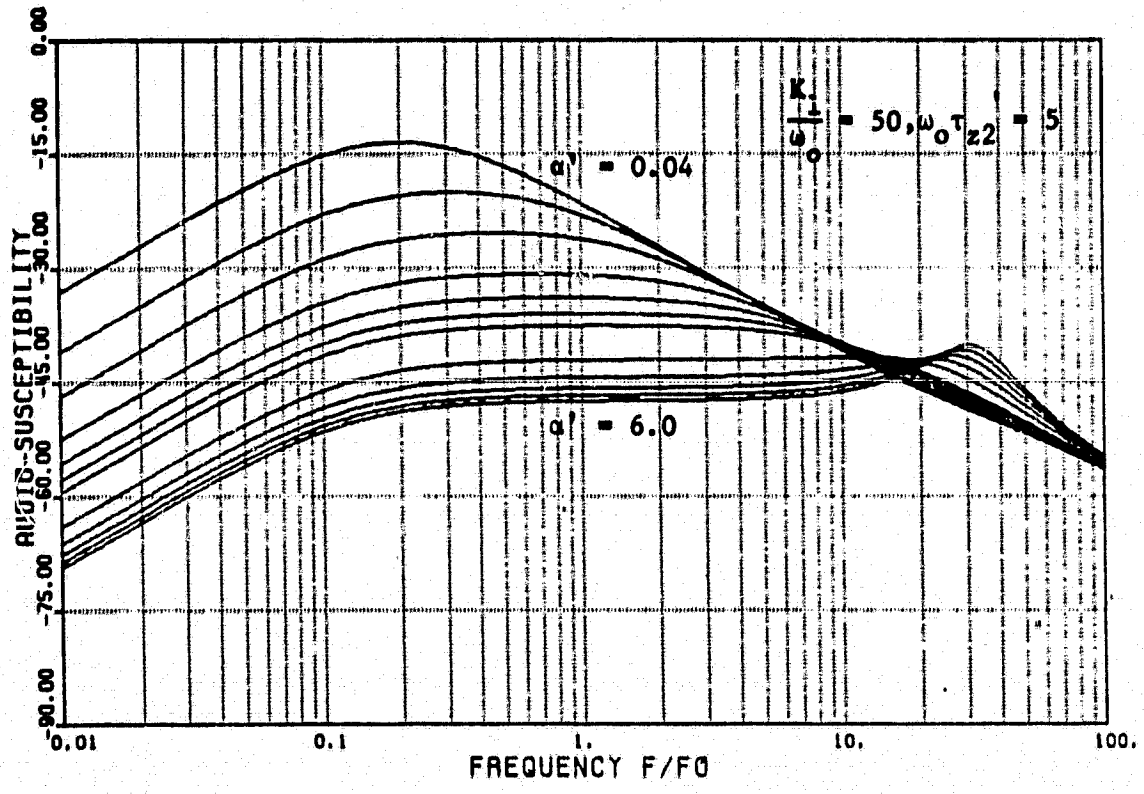


FIG. 3.6 AUDIOSUSCEPTIBILITY CHARACTERISTIC OF A BUCK/BOOST CONVERTER.

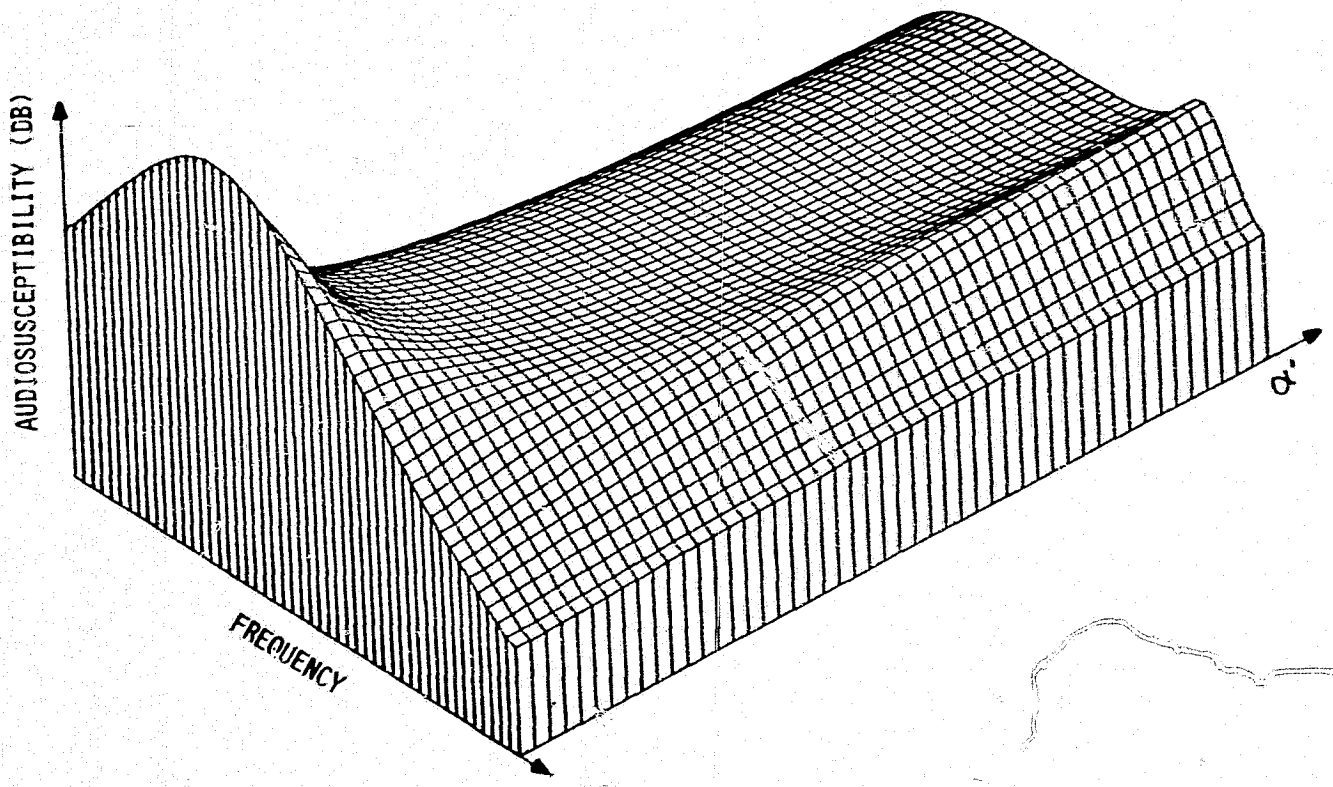


FIG. 3.7 THREE-DIMENSIONAL PLOT OF THE $G_A(s)$ CHARACTERISTIC SHOWN IN FIG. 3.6

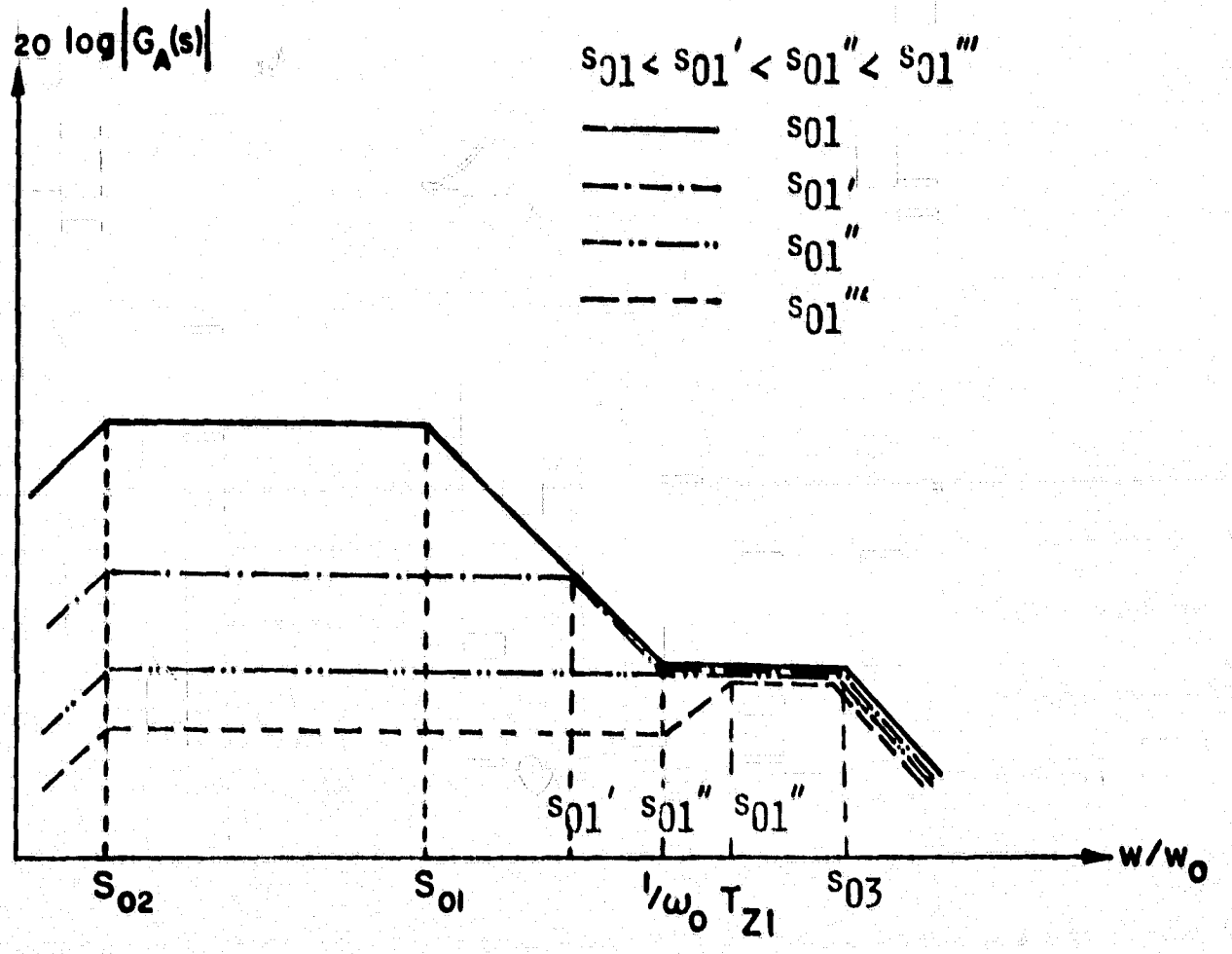


FIG. 3.8 ASYMPTOTIC CURVES OF $G_A(s)$ AS A FUNCTION OF THE CONTROL PARAMETER S_{01}

Case I: $s_{o1} < 1/(\omega_o \tau_{z1})$

The maximum $|G_A(s)|$ occurs at low frequencies between s_{o1} and s_{o2} In the frequency range of interest, it is adequate to assume that

$$|G_T(s)| >> 1$$

and eq. (3.26) can be simplified as

$$G_A(s) = \frac{\omega_o K_2}{\alpha K_1} \frac{s(\tau_{z1}\omega_o s + 1)}{(\frac{s}{s_{o1}} + 1)(\frac{s}{s_{o2}} + 1)} \tag{3.28}$$

$$|G_A(s)|_{max} \approx \frac{\omega_o K_2}{\alpha K_1} s_{o2} = \frac{\omega_o K_2}{K_1 s_{o1}} \frac{\alpha'}{\alpha} \tag{3.29}$$

where $s_{o2} < s < s_{o1}$

It should be noted that equation (3.29) is only a low frequency approximation. Such an approximation is adequate for all practical purposes, since the worst case of audiosusceptibility usually occurs at low frequencies. Equation (3.29) implies that the audiosusceptibility can be improved by increasing the magnitude of s_{o1}. The improvement is expected since increasing the magnitude of s_{o1} results to higher gain-bandwith product of the open-loop characteristics as discussed in the previous section.

Case II: $s_{o1} > 1/(\omega_o \tau_{z1})$

As s_{o1} continues to increase and surpasses the zero, $-1/(\omega_o \tau_{z1})$, caused by the output filter ESR, the audiosusceptibility can no longer be improved and in fact it becomes worsened due to possible peaking effect. A maximum value of $G_A(s)$ characteristic occurs at a frequency higher than that of s_{o1}.

$$|G_A(s)|_{max} = \frac{\omega_o^2 K_2 \alpha'}{K_1 \alpha} \tau_{z1} = \frac{K_2}{K_1} \frac{R_c}{L_e} \frac{\alpha'}{\alpha} \quad , \quad \frac{1}{\omega_o \tau_{z1}} < s < s_{o3} \tag{3.30}$$

Under this condition, the high frequency peaking effect is often observed. When such an effect is considered, the $\max|G_A(s)|$ is generally greater than that indicated in eq. (3.30).

Based on the above described two cases, the best audiosusceptability performance can be obtained under the following condition

$$s_{o1} = \frac{1}{\omega_o \tau_{z1}} \tag{3.31}$$

$$\min \{|G_A(s)|_{max}\} = \frac{K_2}{K_1} \frac{R_c}{L_e} \frac{\alpha'}{\alpha} \tag{3.32}$$

If s_{o1} is approximated by $\alpha' \omega_o \tau'_{z2}$, equation (3.31) yields the condition

$$\alpha' \tau'_{z2} = \frac{L_e}{R_c} \tag{3.33}$$

Equation (3.33) provides the upper limit for the product $\alpha' \tau'_{z2}$.

The output filter capacitor ESR varies over a wide range due to the temperature change. For example, the ESR of a Tantulum capacitor has the following temperature dependant relationship:

$$R_c(-30°c) \approx (3 \text{ or } 4) \cdot R_c(25°c)$$

Therefore, some common sense should be used to determine the upper limit of $\alpha' \tau'_{z2}$ for a specific design.

3.5 Output Impedance Analysis

The converter response to a sinusoidal disturbance of the output current can be investigated by using the output impedance characteristic. The output impedance is measured as the ratio of $\hat{v}_o(s)/\hat{i}_o(s)$, where $\hat{i}_o(s)$ is the sinusoidal disturbance at the converter output. The output impedance characteristic of an open-loop regulator usually has its maximum value at the output filter resonant frequency. The undesirably large output impedance can be reduced effectively by properly designing the control loop paramenters of the SCM.

The closed-loop output impedance can be derived using the small signal model of Fig. 1.2 with $\hat{v}_i(s) = 0$.

$$\frac{\hat{v}_o(s)}{\hat{i}_o(s)} = Z_o(s) = \frac{Z_p(1 + F_M F_1 F_3 F_{AC}) + F_D F_P F_3 F_4 F_{AC} F_M}{1 + G_T} \tag{3.34}$$

Substituting F's of Table 3.1 into (3.34)

$$Z_o(s) = K_3 \frac{\omega_o \tau_{z1} S + 1}{(S^2 + 2\zeta S + 1)(1 + G_T(s))} \left[\frac{\omega_o L_e}{K_3} S + 1\right] \tag{3.35}$$

where

$$K_3 = R_{eq} + \frac{2V_I L_e}{M} \approx \frac{2V_I L_e}{M} = K_1 L_e \tag{3.36}$$

Comparing (3.35) with (3.26), the analytical expressions for $G_A(s)$ and $Z_o(s)$ are similar except for an additional high frequency zero, $-K_3/(\omega_o L_e)$, for the $Z_o(s)$ characteristic. High frequency peaking phenomenon for sufficiently large α' similar to that described in the previous section is illustrated in Fig. 3.9.

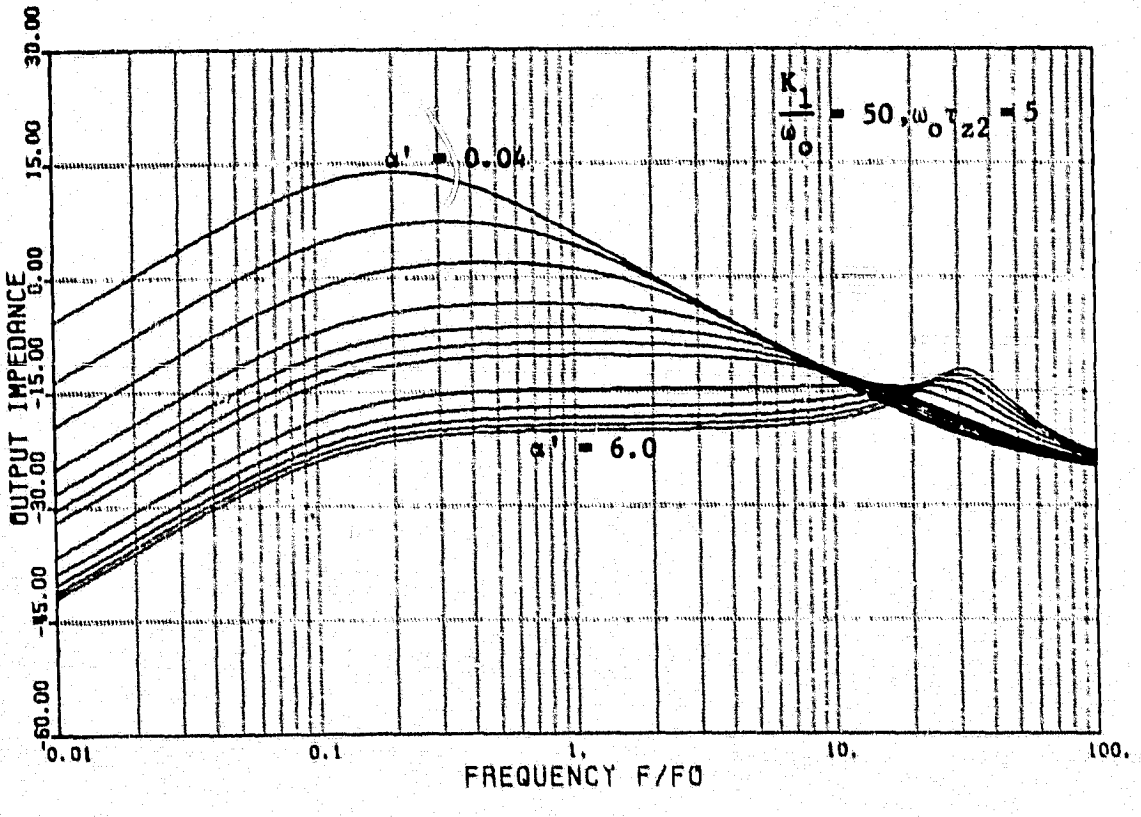


FIG. 3.9 THE OUTPUT IMPEDANCE CHARACTERISTIC

The following two cases are examined:

Case 1: $s_{o1} < 1/(\omega_o \tau_{z1})$

Equation (3.35) can be simplified if one assumes that K_1 is sufficiently large and the zero $-K_3/(\omega_o L_e)$ has insignificant effect in the low frequency range. Equation (3.35) can be simplified for low frequency approximation as

$$Z_o(s) = \frac{\omega_o L_e}{\alpha} \frac{s(\tau_{Z1}\omega_o s + 1)}{(\frac{s}{s_{o1}} + 1)(\frac{s}{s_{o2}} + 1)} \tag{3.37}$$

Comparing (3.37) with (3.28), the simplified output impedance characteristic is almost the same as that of the audiosusceptibility characteristic, except that the dc gain is different.

The maximum output impedance occurs at a frequency between s_{o1} and s_{o2}

$$|Z_o(s)|_{max} = \frac{\omega_o L_e}{\alpha} s_{o2} = \frac{L_e}{\alpha \tau'_{Z2}} \tag{3.38}$$

Case II: $s_{o1} > \frac{1}{\omega_o \tau_{Z1}}$

Similar to *Case* II of the previous section, the maximum output impedance occurs at a frequency higher than that of $1/(\omega_o \tau_{Z1})$

$$\min \left\{ |Z_o(s)|_{max} \right\} = R_c \frac{\alpha'}{\alpha} \tag{3.39}$$

Equation (3.39) imposes the theoretical limit of the output impedance which is determined primarily by the output filter capacitor ESR. (The ratio of α'/α is close to one for all practical concerns.) Of course, the high frequency peaking is likely to occur in this case and the maximum $|Z_o(s)|$ can be worse than that indicated by (3.39) should *Case* II prevail.

3.6 Transient Response Due to a Step Load Change.

The converter load is often subjected to step load changes. Undesireable resonance between the load and the regulator due to these load changes may result in excessive disturbances of the output voltage. For this reason, the time constant of the transient responses and the amount of allowable peaking are specified for each application. If the load charge is not a severe one, such as a sudden short at the output, the output voltage and duty cycle of the converter usually change only slightly during the entire transient. The output impedance derived in the previous section for the small signal model can be used to examine the transient response of the converter. For a step change of the load current $\Delta I_o/s$, equation (3.37) can be rewritten with an unnormalized s as

$$\hat{v}_o(s) = \Delta I_o \omega_o^2 L_e \frac{\alpha'}{\alpha} \left[\frac{B_1}{s + s'_{o1}} + \frac{B_2}{s + s'_{o1}}\right] \tag{3.40}$$

where

$$s'_{o1},\ s'_{o2} = \frac{\alpha' \tau'_{z2} \omega_o^2}{2} \left[1 \pm \sqrt{1 - \frac{4\alpha'}{(\alpha' \tau'_{z2} \omega_o)^2}}\right] \tag{3.41}$$

$$B_1 = \frac{-\tau_{z1} s'_{o1} + 1}{-s'_{o1} + s'_{o2}} \tag{3.42}$$

$$B_2 = \frac{\tau_{z1} s'_{o1} - 1}{-s'_{o1} + s'_{o2}} \tag{3.43}$$

Taking the inverse Laplace transform of eq. (3.40) results in the time transient response as a sum of two exponential terms:

$$\Delta V_o(t) = \Delta I_o \frac{\alpha'}{\alpha} \omega_o^2 L_e \left[B_1 e^{-s'_{o1} t} + B_2 e^{-s'_{o2} t}\right] \tag{3.44}$$

The transient response of the output voltage is illustrated in FIg. 3.10. The settling time and the peaking can be determined analytically from (3.44). The time constant of the transient response is usually dominated by the second term of (3.44) since for all practical designs the two corner frequencies are sufficiently apart and $s'_{o1} >> s'_{o2}$ as suggested in earlier sections. However, if s'_{o1} and s'_{o2} form a complex conjugate pair, the transient response will be oscillatory instead of exponentially decaying. For an illustration of the latter case, please refer to Fig. 9.8. of Volume I.

The peaking of ΔV_o during the load transient can also be derived from (3.44). As a first order approximation, it is reasonable to assume $s'_{o1} >> s'_{o2}$. Therefore, the peaking magnitude can be approximated by

$$|\Delta V_o(t)|_{max} = \frac{\Delta I_o L_e}{\alpha \tau'_{z2}} \tag{3.45}$$

Employing eq. (3.38), one can express (3.45) by the following equation

$$|\Delta V_o|_{max} = \Delta I_o |z_o|_{max} \tag{3.46}$$

$$A_1 = \Delta I_o \frac{\alpha'}{\alpha} \omega_o^2 L_e \quad B1$$

$$A_2 = \Delta I_o \frac{\alpha'}{\alpha} \omega_o^2 L_e \quad B2$$

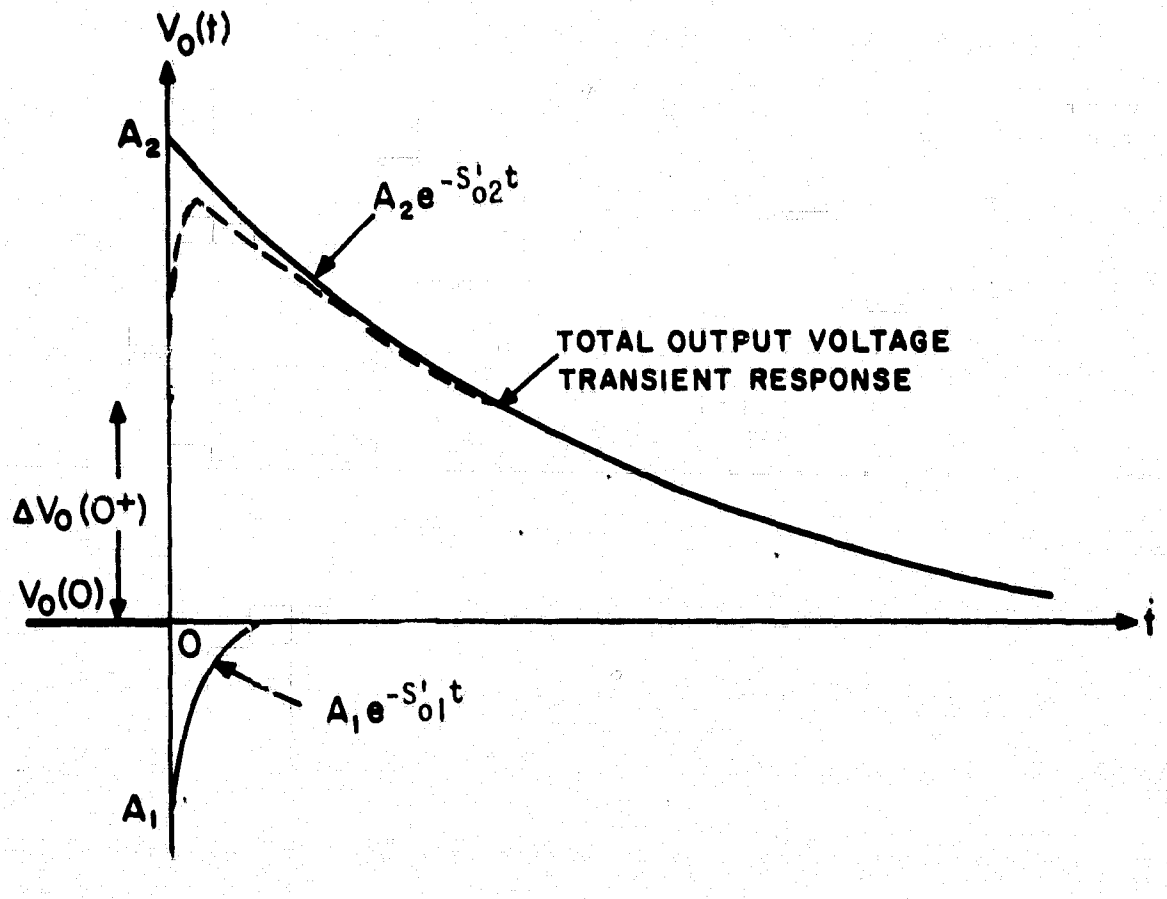


FIG. 3.10 THE OUTPUT VOLTAGE TRANSIENT RESPONSE DUE TO OUTPUT CURRENT STEP CHANGE

3.7 DC Regulation

The operational amplifier transfer function A(s) can be expressed as

$$A(s) = \frac{K}{1 + \frac{s}{\omega_o}}$$

where K is the DC gain. A typical value for K is 10^5. The gains $F_{AC}(s)$ and $F_{DC}(s)$ shown in Table 3.1 can be expressed as

$$F_{AC}(o) = K \frac{R_x + R_3}{R_x + R_3 + R_4} \tag{3.47}$$

where $R_x = R_1 || R_2$

$$F_{DC}(o) = \frac{K}{R_y} [R_4 || (R_x + R_3)]$$

where

$$R_y = \frac{R_x + R_3}{g} \tag{3.48}$$

and

$$g = \frac{R_2}{R_1 + R_2}$$

Substituting (3.47) and (3.48) into the open loop gain $G_T(s)$ and letting s = 0, one obtains

$$G_T(o) = F_M \cdot F_D(o)\, F_{DC}(o)$$

$$= \frac{2R_4C_1}{nM} K \frac{gR_x}{R_x + R_3 + R_4} F_D(o) \tag{3.49}$$

where

$$F_D(o) = \frac{V_o}{D} \qquad \cdots\cdots \text{ Buck}$$

$$= \frac{V_o}{D'}\left(1 - \frac{R_e}{R_L}\right) \quad \cdots\cdots \text{Boost}$$

$$= \frac{V_o}{DD'}\left(1 - D\,\frac{R_e}{R_L}\right) \quad \cdots\cdots \text{Buck/Boost}$$

$$G_A(o) = \frac{\Delta V_o}{\Delta V_I} = \frac{F_I(o)F_p(o)}{1 + G_T(o)} \approx \frac{F_I(o)}{G_T(o)}$$

$$= \left(F_M K\,\frac{gR_4}{R_4 + R_x}\right)^{-1} \frac{F_{I(o)}}{F_D(o)} \qquad (3.50)$$

where

$$\frac{F_I(o)}{F_D(o)} = \frac{D}{V_I} \quad \cdots\cdots \text{Buck}$$

$$= \frac{D'}{V_I\left(1 - \frac{R_e}{R_L}\right)} \quad \cdots\cdots \text{Boost} \qquad (3.51)$$

$$= \frac{DD'}{V_I\left(1 - \frac{R_e}{R_L}\right)} \quad \cdots\cdots \text{Buck/Boost}$$

The DC regulation is expressed as a percentage change of the output voltage with respect to its nominal value.

$$\frac{\Delta V_o}{V_o} = \left(F_M K\,\frac{gR_4}{R_4 + R_x}\right)^{-1} \frac{F_I(o)}{F_D(o)}\,\frac{\Delta V_I}{V_o} \qquad (3.52)$$

3.8 Summary

It is commonly known that the performance characteristics of the three converters, buck, boost, and buck/boost, are quite different, primarily due to the non-minimum phase property (a zero on the right-half s-plane) that exists in the boost and buck/boost converters but not in the buck converter. The existence of a zero on the right-half s-plane, and two moving poles, have caused the boost and buck/boost converters to be more susceptible to loop instability.

It is quite astonishing to discover that the performance characteristics of all three switching regulator types share a common form when SCM control is employed. As discussed in Chapter 10 of Volume I, the SCM control is not only capable of moving the zero in the right-half s plane to the left-half s plane, but also of adaptively compensating the two moving poles of the boost and buck/boost converters. This analytical finding has a significant design impact: A simple unified design procedure can be devised for all three regulator types such that all regulator performance specifications can be satisfied concurrently in one design attempt.

CHAPTER IV

INPUT FILTER EFFECTS

4.1. Introduction.

An input filter is often required between a switching regulator and its power source. The filter serves to prevent the regulator switching current from being reflected back into the source, and 2) to isolate source-voltage transients so as not to degrade the performance of the switching regulator downstream. Consequently, the filter is required to provide not only high attenuation at the switching frequency, but also sufficient damping against any line disturbance so that output peaking is properly controlled. A presumably well-designed input filter, satisfying the aforementioned requirements, when married to a switching regulator, can often cause significant performance degradations. These degradations are due primarily to the complex interaction between input-filter, output-filter, and control loop [11-13], and result in various design problems which include: 1) the destablizing interactions between an improperly designed input-filter and the regulator loop, 2) the detrimental effect of input-filter resonant peaking on the closed-loop input-to-output transfer characteristic of the switching regulator (commonly referred to as the audiosusceptibility performance), and 3) the ever-present weight and loss limitations placed on the input-filter.

The objective of the present chapter is to investigate the interactions between the control loop and the power stage in the presence of an input filter and to incorporate input filter effect into the SCM design guidelines.

4.2 Switching Regulator Model With An Input-Filter.

The effect of the input-filter is characterized by the forward transfer characteristic of the input filter, $H_F(s)$, and the output impedance of the input-filter, $Z_F(s)$, as shown in Fig. 4.1. The common block diagram shown in Fig. 1.2 is applicable for a switching regulator with an input-filter if the following modifications of the transfer functions $F_I(s)$, $F_D(s)$ and $F_p(s)$, (reference to Volume I for details), are made:

$$F_I'(s) = \frac{1}{\mu} H_F(s)$$

where $\mu = \frac{1}{D}$

$= D'$

$= \frac{N_P}{N_S} \frac{D'}{D}$

$$F_D'(s) = \frac{V_o}{D}\left(1 - \frac{Z_F(s)}{\mu^2 R_L}\right) \quad \text{..... Buck}$$

$$= \frac{V_o}{D'}\left[\left(1 - \frac{R_e + s\omega_o L_e}{R_L}\right) - \frac{Z_F(s)}{\mu^2 R_L}\right] \quad \text{..... Boost}$$

$$= \frac{V_o}{DD'}\left[\left(1 - D\frac{R_e + s\omega_o L_e}{R_L}\right) - \frac{Z_F(s)}{\mu^2 R_L}\right]$$

and ..... Buck/Boost

(4.1) (4.2)

$$F_p'(s) = \frac{\left(R_c + \frac{1}{s\omega_o C}\right) || R_L}{Z_F(s) + Z_i(s)} \frac{1}{\omega_o^2} \qquad (4.3)$$

where $Z_i(s) = R_{eq} + s\omega_o L_e + \left(R_c + \frac{1}{s\omega_o c}\right) || R_L$

$Z_i(s)$ is the input impedance of the equivalent output filter of the power stage.

$H_F(S)$: THE FORWARD TRANSFER CHARACTERISTIC

$Z_F(S)$: THE OUTPUT IMPEDANCE OF THE INPUT FILTER

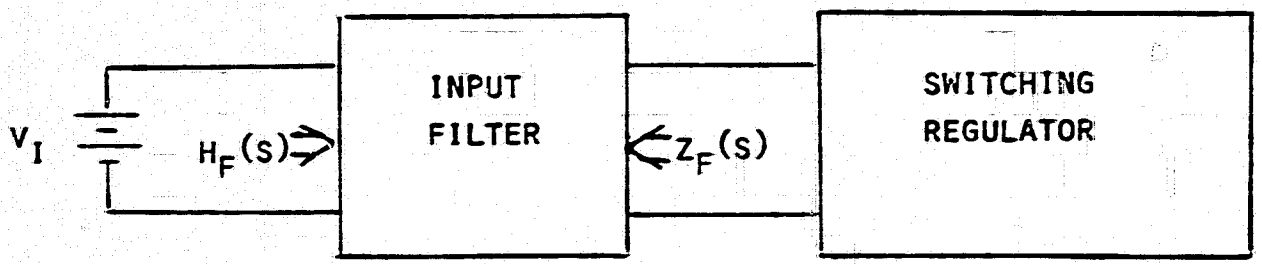


FIG. 4.1 BLOCK DIAGRAM OF A SWITCHING REGULATOR WITH AN INPUT FILTER

4.3. Input Filter Interactions.

Employing the small-signal linear model shown in Fig. 1.2, interactions among input filter, output filter, and control loop are investigated.

A. Loop Stability The stability of a switching regulator can be examined by the open-loop gain $G_T(s)$ of eq. (3.12). The input-filter design parameter central to the loop gain is the output impedance $Z_F(s)$ which affects the transfer function $F'_D(s)$ and $F'_p(s)$.

1) The output impedance $Z_F(s)$ is related to the duty-cycle power-stage gain F'_D through equation (4.2). It is interesting to point out that $\mu^2 R_L$ is the absolute value of the negative impedance of a switching regulator at a given operating condition. As a necessary condition for stability, the magnitude of the output impedance of an input filter should not be greater than the absolute value of the negative impedance of the regulator.

$$\left| Z_F(j\frac{\omega_1}{\omega_o}) \right| < \mu^2 R_L \qquad (4.4)$$

Excessive output impedance $Z_F(s)$ at the resonant frequency of the input filter can result in a negative duty-cycle power-stage gain. The negative duty-cycle power-stage gain $F'_D(s)$ together with the negative feedback loop will contribute to an unstable positive feedback system.

Figure 4.2 illustrates the Bode plot of the amplitude of $F'_D(s)$. The effect of the resonant peaking of $Z_F(s)$ results in an abrupt reduction of $F'_D(s)$ at the resonant frequency ω_1. For boost or buck/boost

converter, the input filter resonant frequency ω_1 can occur before the positive zero (shown in Fig. 4.2(b)) or after the positive zero (shown in Fig. 4.2(c)). Since the positive zero usually occurs at high frequencies, the case shown in Fig. 4.2(c) is seldom encountered for most practical designs.

2) The output impedance is related to the power stage transfer function $F'_p(s)$ through equation (4.3). Excessive $Z_F(s)$ at the resonant frequency can significantly reduce $F'_p(s)$, and therefore, the loop gain. The following relation should be observed

$$\left|Z_F(s)\right| << \left|Z_i(s)\right| \quad \text{for all s.} \tag{4.5}$$

The degration of $F'_p(s)$ due to $Z_F(s)$ can be avoided, if there is a sufficient separation of the input-filter resonant frequency $\omega_1 \triangleq 1/\sqrt{L_1C_1}$, and the output filter resonant frequency $\omega_o \triangleq 1\sqrt{LC}$. Fig. 4.3(a) shows that a maximum interaction occurs between the input-filter and the output-filter when ω_1 coincides with ω_o. This interaction can result in a large reduction of $F'_p(s)$. Such interaction can be minimized by either decreasing ω_1 or increasing ω_1, as shown in Fig. 4.3(b) and (c). Larger ω_1 is desirable from the point of view of weight and size reduction. However, for higher resonant frequency ω_1, the effect of the peaking of $Z_F(s)$ becomes more prominent since the loop gain descends rapidly as frequency increases.

Figure 4.4 illustrates the open-loop gain and phase plot of a buck/boost regulator with the same circuit parameter values employed in Fig. 3.3. The filter parameters are $L_1 = 77\mu H$, $R_1 = 39.6m\Omega$, and C1 = 412 f, which gives an exaggerated $\left|Z_F(j\omega_1)\right| = 4.75\Omega$ and $\left|H_F(j\omega_1)\right| = 11$

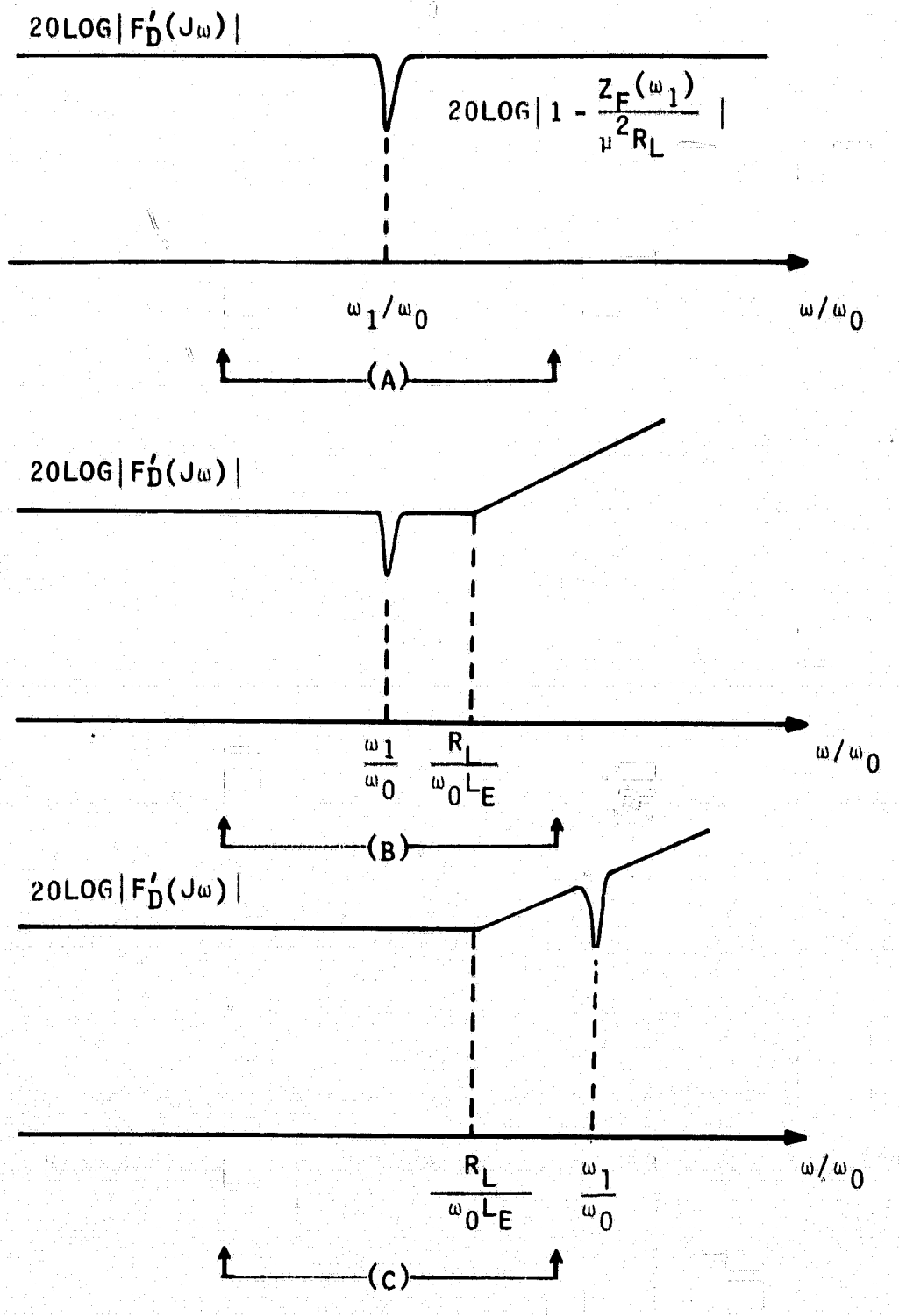


FIG. 4.2 BODE PLOT FOR $|F_D(J\omega)|$ FOR (A) BUCK CONVERTER (B) BOOST OR BUCK/BOOST THE INPUT FILTER RESONANT FREQUENCY ω_1 LESS THAN THE POSITIVE ZERO $\frac{R_L}{\omega_0 L_E}$

(C) ω_1 GREATER THAN THE POSITIVE ZERO

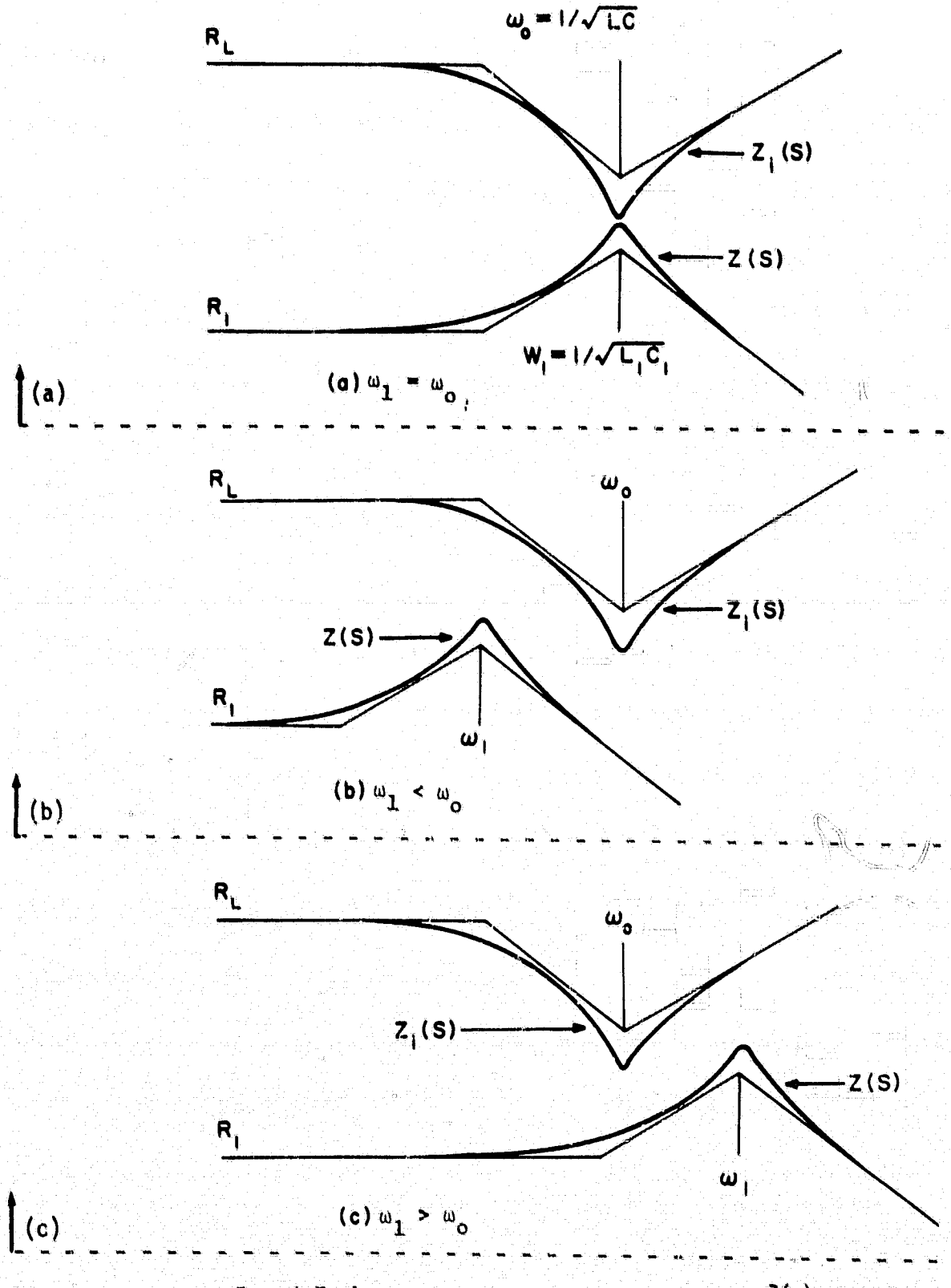


FIG. 4.3 INTERACTION BETWEEN OUTPUT IMPEDANCE Z(s) OF INPUT FILTER AND INPUT IMPEDANCE $Z_1(s)$ OF REGULATOR

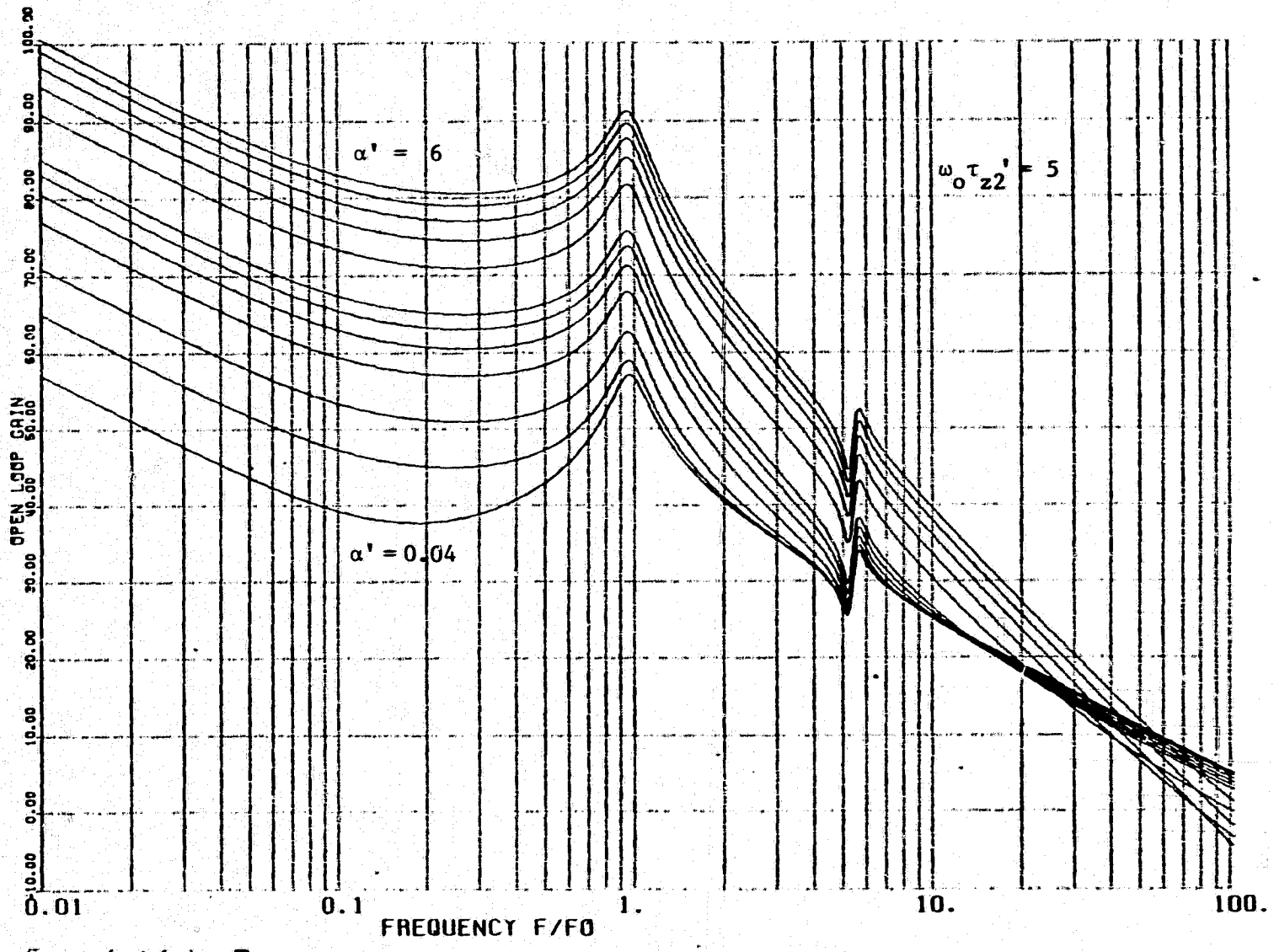


FIG. 4.4(A) THE EFFECT OF THE INPUT FILTER ON THE OPEN LOOP CHARACTERISTIC (GAIN) OF A BUCK/BOOST CONVERTER

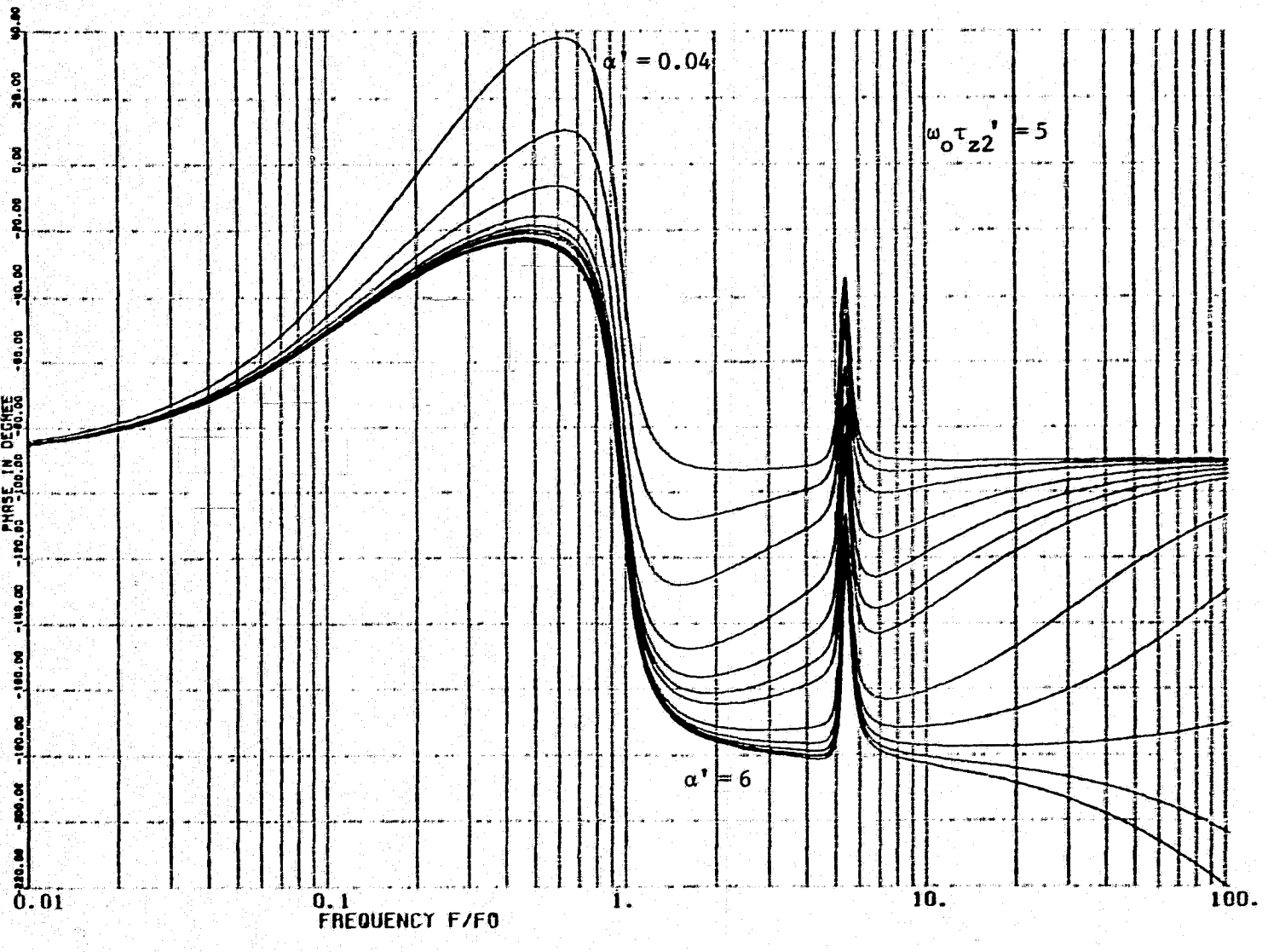


FIG. 4.4(B) THE EFFECT OF THE INPUT FILTER ON THE OPEN LOOP CHARACTERISTIC (PHASE)

at the resonant frequency $\omega_1 = 1/\sqrt{L_1C_1}$ to demonstrate the effect of an input filter. It is interesting to note that although there is a significant gain and phase disturbance at the input filter resonant frequency, the open loop characteristics in the neighborhood of the cross-over frequencies are rather unperturbed due to the high-gain wide-bandwidth nature of the open-loop characteristics. Therefore, the loop instability due to the input filter interaction is much alleviated with SCM control.

B. Audiosusceptibility. The audiosusceptibility is expressed as

$$G_A'(s) = \frac{F_I'(s)F_p'(s)\ [1+F_1(s)F_3(s)F_{Ac}(s)F_M(s)]}{1 + G_T'(s)} \tag{4.6}$$

The forward transfer function $H_F(s)$ is related to the transfer function $F_I'(s)$ as shown in equation (4.1). Execessive peaking of $H_F(s)$ can result in severe degradation of the audiosusceptibility of the regulator. Figure 4.5 illustrates the audiosusceptibility of a buck/boost converter with an input filter for different values of α'. For $\alpha' = 1$, approximately 23 dB of peaking is observed, compared to 21 dB calculated using (4.1) thus accounting for the effect of $H_F(s)$ in the transfer function $F_I'(s)$. The particular peaking effect at very high frequency discussed in Volume I is not important in the audiosusceptibility characteristic since it is largely attenuated by the input filter.

The maximum value of $G_A'(s)$ due to peaking at resonant frequency is defined to be $\left|G_A'(jw_1)\right|_{max}$ and is calculated as follows.

$$\text{Let} \quad K_F = \frac{Z_F(jw)}{\mu^2 R_L} \tag{4.7}$$

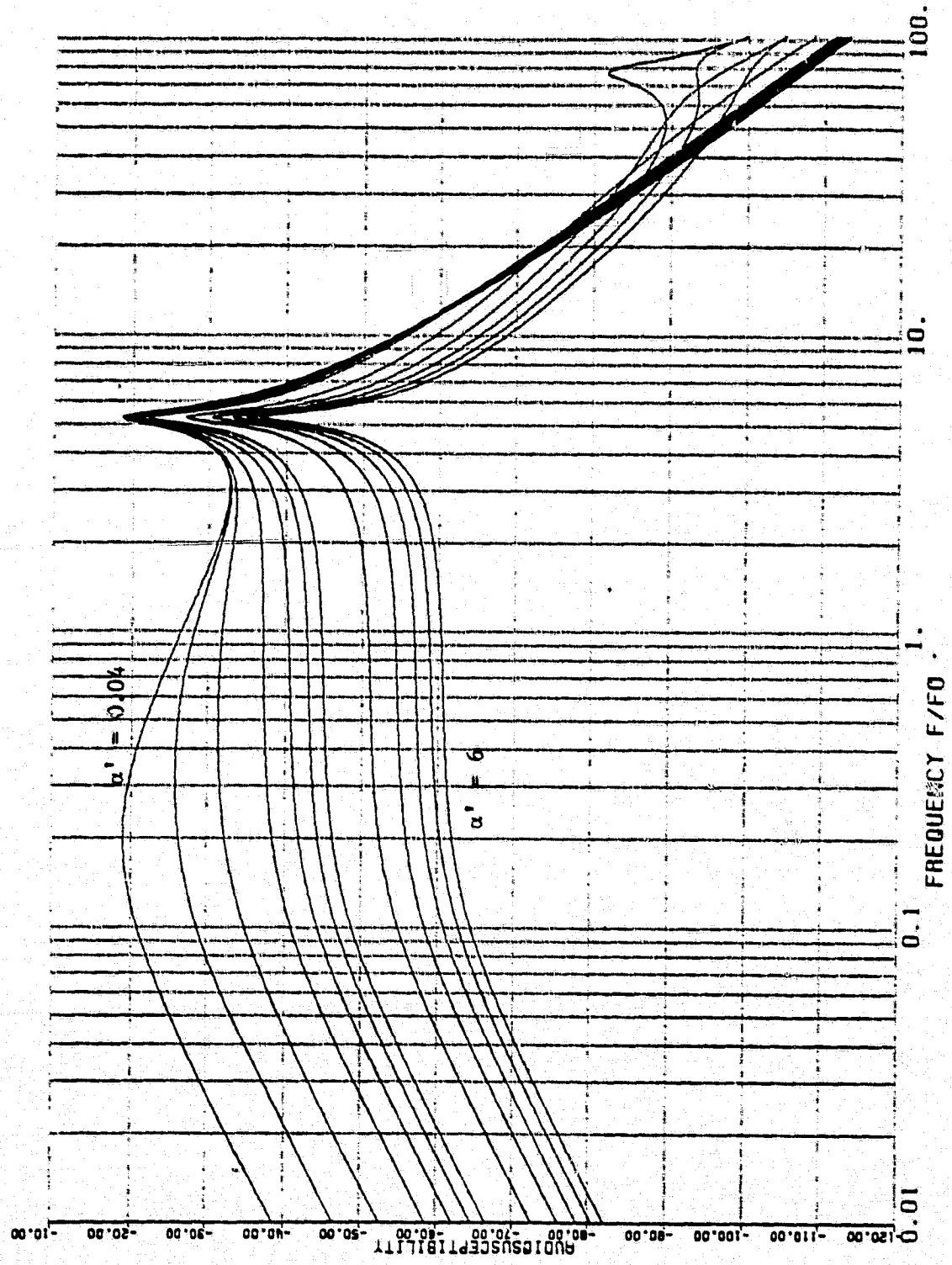


FIG. 4.5 THE EFFECT OF THE INPUT FILTER ON THE AUDIO-SUSCEPTIBILITY CHARACTERISTIC

Then open loop gain can be expressed as

$$G_T'(s) = K_1 \frac{\alpha}{\omega_o s} \frac{1 - K_F}{1 + K_F} \frac{\frac{1}{\alpha'} s^2 + \tau_{z2}' s + 1}{\frac{1}{1+K_F} s^2 + \frac{2\zeta}{1+K_F} s + 1} \tag{4.8}$$

Assuming that the open loop gain at the input filter resonant frequency ω_1 is sufficiently large, i.e.

$$|G_T'(j\omega_1)| >> |$$

Then for low frequency approximation

$$G_A'(s) \simeq \frac{F_I' F_P'}{G_T'(s)} [1 + F_2 F_3 F_{AC} F_M]$$

$$= \frac{H_F(s)}{1 - K_F} \cdot \frac{\omega_o K_2}{\alpha K_1} \frac{s(\tau_{z1}\omega_o s + 1)}{(\frac{s}{s_{o1}} + 1)(\frac{s}{s_{o1}} + 1)}$$

$$= \frac{H_F(s)}{1 - K_F} [G_A(s)]_{\omega/o \text{ input filter}} \tag{4.9}$$

If the input filter resonant frequency satisfied the relationship,

$$|s_{o2}| < |\frac{\omega_1}{\omega_o}| < |s_{o1}| \tag{4.10}$$

the desired $\left| G_A'(j\omega_1) \right|_{max}$ is given by the equation

$$|G_A'(j\omega_1)|_{max} \simeq \frac{B_F}{1 - \frac{B_R}{\mu^2 R_L}} \cdot |G_A(j\omega_1)| \quad \text{without an input filter} \tag{4.11}$$

In equation (4.11), B_F is defined to be the peaking of the input filter forward transfer characteristic, and B_R is defined to be the peaking of the output impedance of the input filter. B_F and B_R are given by the expressions

$$\left.\begin{aligned} B_F &= |H_F(j\omega_1)| \\ B_R &= |Z_F(j\omega_1)| \end{aligned}\right\} \tag{4.12}$$

It is evident from (4.11) that a substantial amount of input filter peaking (high B_F and/or B_R) would result in severe degradation of the audio-susceptibility of a converter.

C. Output Impedance Characteristic. The output impedance characteristic is illustrated in Fig. 4.6 for different values of α'. The input filter interaction is less noticeable here than in the audiosusceptibility or the open loop characteristics because the output impedance of the power stage, $Z_p(s)$, is less sensitive to the input filter peaking effect. For all practical purposes, the effect of the input filter on the output impedance characteristic can be neglected for SCM controlled regulators.

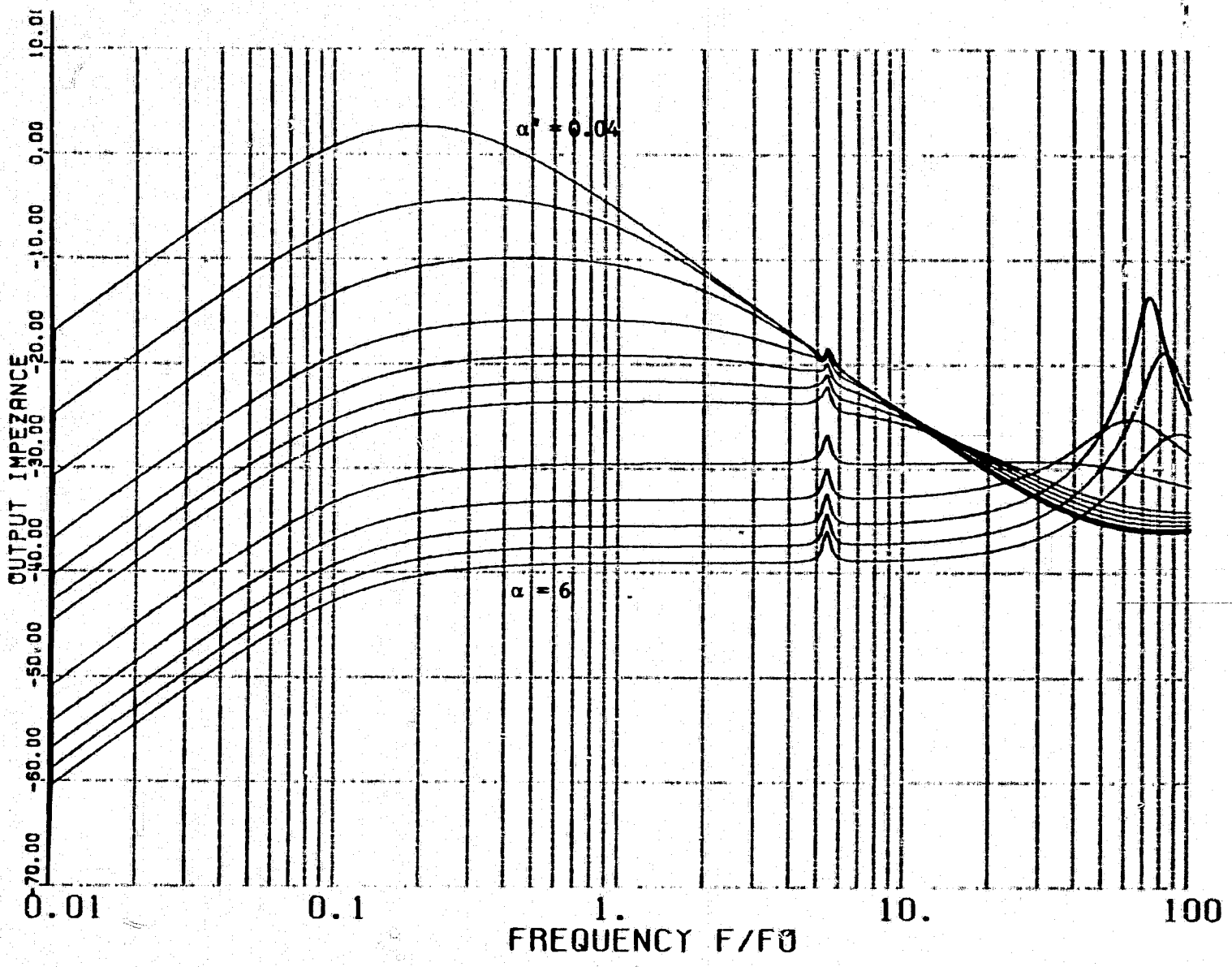


FIG. 4.6 THE EFFECT OF THE INPUT FILTER ON THE OUTPUT IMPEDANCE CHARACTERISTIC

4.4 Input Filter Design Considerations

One can conclude that the minimization of $Z_P(s)$ and $H_P(s)$ at filter resonance is the key to designing an input filter for a switching regulator with a given power stage, and specified line and load conditions.

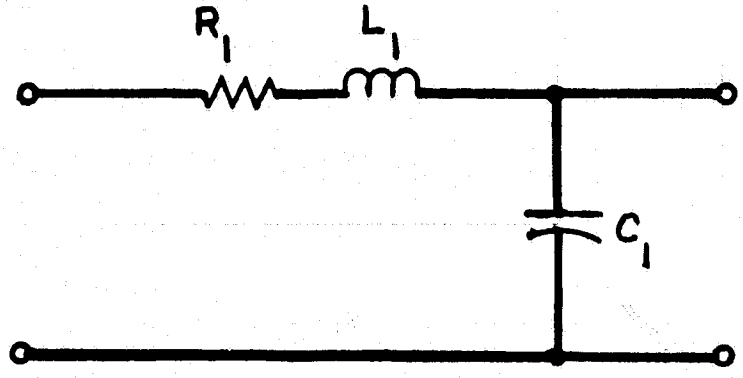
In conventional single-stage input-filter design, the performance degradations are often compensated by using a larger filter L and C, or by using an externally added R in series with filter L or C to bring the resonant peaking under control. In any case, the designer has to suffer the penalty of increased size, weight, and loss. A satisfactory filter design becomes rather difficult to achieve without trading one or more performance characteristics for size, weight, or efficiency.

An optimum, two-stage input-filter configuration as shown in Fig. 4.7 was described in detail [11-13]. This filter configuration is capable of providing low-loss, light-weight, high-attenuation, and a controlled resonant peaking of $H_F(s)$ and $Z_F(s)$. The filter is particularly useful for switching regulators which have stringent efficiency, attenuation, and peaking requirements, and which would fail to meet size and weight requirements if a conventional, single-stage filter were used.

4.5. Input Filter Related SCM Design Guidelines.

High-gain and wide-bandwidth is one of the intrinsic characteristics of switching regulators employing SCM control. Typical open loop cross-over frequency occurs at 1/3 to 1/2 of the switching frequency. Because of the stringent military specifications on conducted interference requirement, the loop gain reduction due to an input filter usually occurs at a frequency approximately a half decade or even a decade prior to the open-loop crossover frequency.

SINGLE-STAGE INPUT FILTER



TWO-STAGE INPUT FILTER

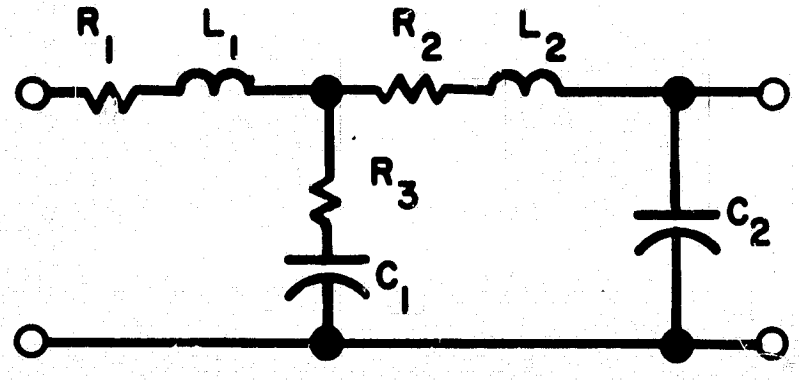


FIG. 4.7 INPUT FILTER CONFIGURATIONS

As a result, gain reduction occurs at a frequency where there is sufficient loop gain and is not likely to cause loop instability. In Fig. 4.4, a poorly designed input filter causes a noticeable gain reduction. This gain reduction, however, occurs a decade earlier than the cross-over frequency and does not cause loop instability. If an input filter is designed with a controlled $Z_F(s)$ peaking less than 20% of the negative impedance $\mu^2 R_L$, and the input filter resonant frequency ω_1 is much less than 1/3 of the switching frequency, the input filter related loop instability can be largely avoided. Therefore, no special attention is given in SMC design to avoiding the loop instability in the presence of an input filter.

The peaking effect of the forward transfer characteristic $H_F(s)$ has significant effect on the audiosusceptibility characteristic of a switching regulator as shown in Fig. 4.5. A sharp spike is seen at the input filter resonant frequency and is primarily contribed by the peaking of $H_F(s)$. This effect will be considered in the SCM design process.

CHAPTER V.

DESIGN ASSUMPTIONS AND CONSTRAINTS

5.1. Introduction.

The philosophy of system design is to establish a simple correlation between the system parameters and the characteristic roots so that the roots may be set at desired locations by adjusting the system parameters. Then the roots are interpreted in terms of the time and frequency response.

In this chapter, the key power stage parameters and SCM parameters are identified. Switching regulator performance specifications are presented in the form of design constraints. The design objective is to determine the set of SCM parameters for given power stage parameters such that the prescribed design constraints could be satisfied and subsequently switching regulator performance optimized.

5.2. Key Design Parameters.

The key design parameters can be divided into the following categories:

(A) key power stage parameters which have already been determined prior to the control circuit design.

(B) key SCM parameters which are the design variables to be determined with given power stage parameters and performance specifications.

These two categories of design parameters are given as follows:

(A) Key power stage parameters.

- Input filter resonant frequency ω_1
- Peaking of the input filter forward transfer characteristic $B_F = |H_F(j\omega_1)|$
- Peaking of the output impedance of input filter $B_R = |Z_F(j\omega_1)|$.

- Equivalent output filter parameters: L_e, R_{eq}, C, R_c, ω_0, ζ. These parameters are defined in section 3.2.
- Output filter $\tau_{Z1} = R_c C$
- Input voltage range, output voltage and duty cycle ranges: V_I, V_0, D and D'
- Negative Resistance of the switching regulator at an operating condition = $\mu^2 R_L$

(B) Key SCM design variables

- Equivalent DC loop resistor R_y
- AC loop resistor R_4
- DC loop time constants: τ_{Z2} and τ'_{Z2}
- Compensation loop time constant: $\tau_{p1} = R_5 C_2$
- Adaptive parameter: α and α'
- Pulse modulator gain $F_M = \frac{2R_4 C_1}{nM}$

The above described parameters are defined earlier in Chapter 3.

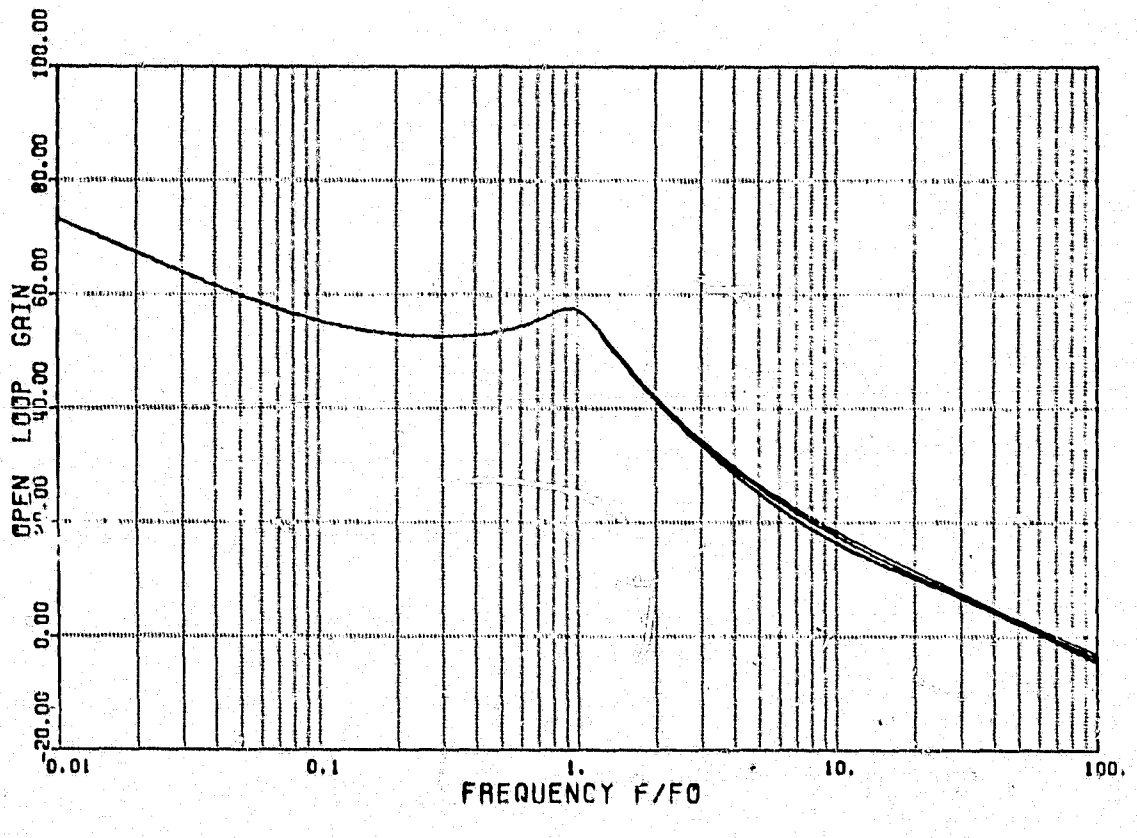
5.3 Design Assumptions.

(1) To simplify the mathematical representation of the open-loop transfer function, it is assumed that the compensation loop parameter τ_{p1} is designed to match τ_{Z1}

$$\tau_{p1} = \tau_{Z1} \tag{5.1}$$

If the above equality constraint is not grossly violated, only minor effects in the overall loop performance will result. Figure 5.1 shows that for different values of R_5, ranging from 500 Ω to 2000 Ω, the open-loop characteristics of a buck/boost converter change very little. The parameter values used for the converter in Figure 5.1 are the same as those used for Figure 3.3. Figure 5.2 shows that if the equality constraint (5.1) is violated by one order of magnitude, the difference in phase delay becomes more discernable.

Fig. 5.3 illustrates the effect of changing output filter ESR. In general, larger phase delays are shown at high frequency as a result of employing either smaller τ_{p1} or larger τ_{Z1}. The mathematical expressions of the open-loop transfer functions, with the inclusion of the effect of τ_{p1} when equation (5.1) is violated, are too complex to render analytical insight. As shown in equations (10.2), (10.3) and (10.4) in Volume I, the order of the transfer functions are increased by one for both the numerator and denominator terms.



(a)

FIG. 5.1 OPEN LOOP CHARACTERISTIC FOR DIFFERENT R_5 (C_2 = 0, 032 μF) R_5 = 500 Ω, 1000 Ω AND 2000 Ω (A) GAIN

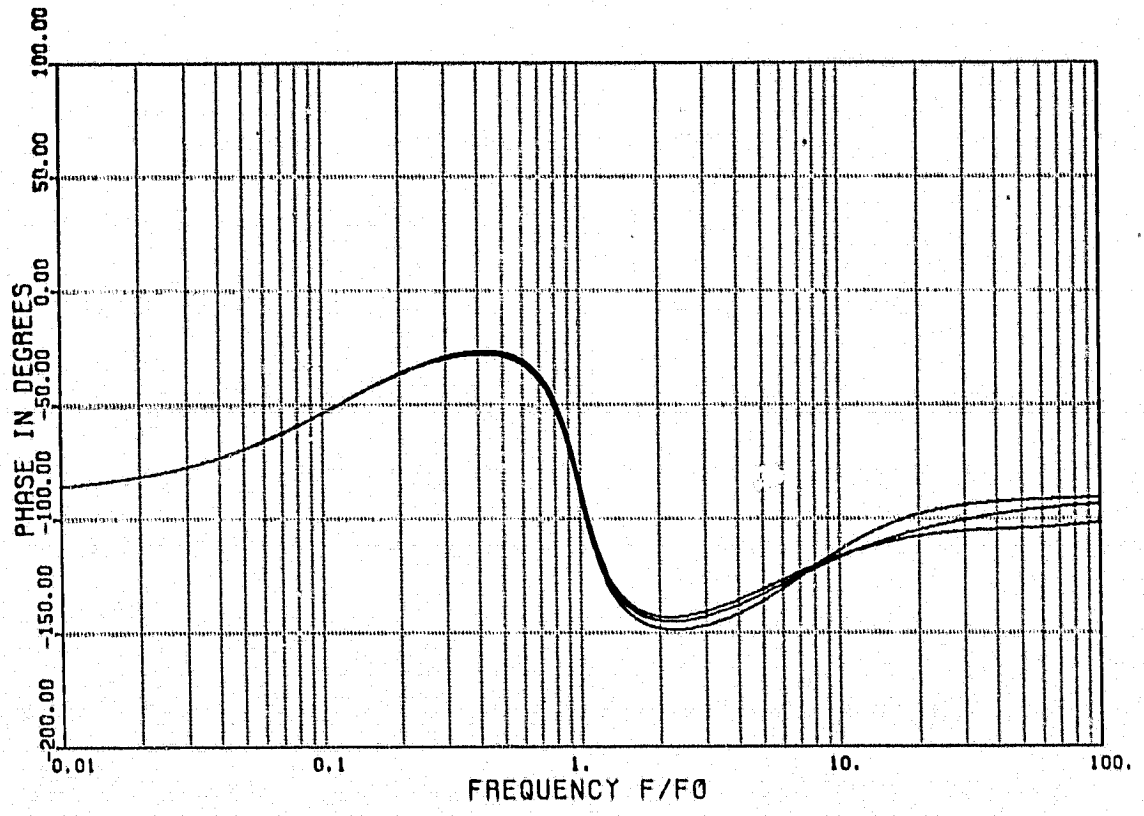


FIG. 5.1 OPEN LOOP CHARACTERISTIC FOR DIFFERENT R_5 (C_2 = 0.032 μF)
R_5 = 500Ω, 1000Ω AND 2000Ω.
(B) PHASE

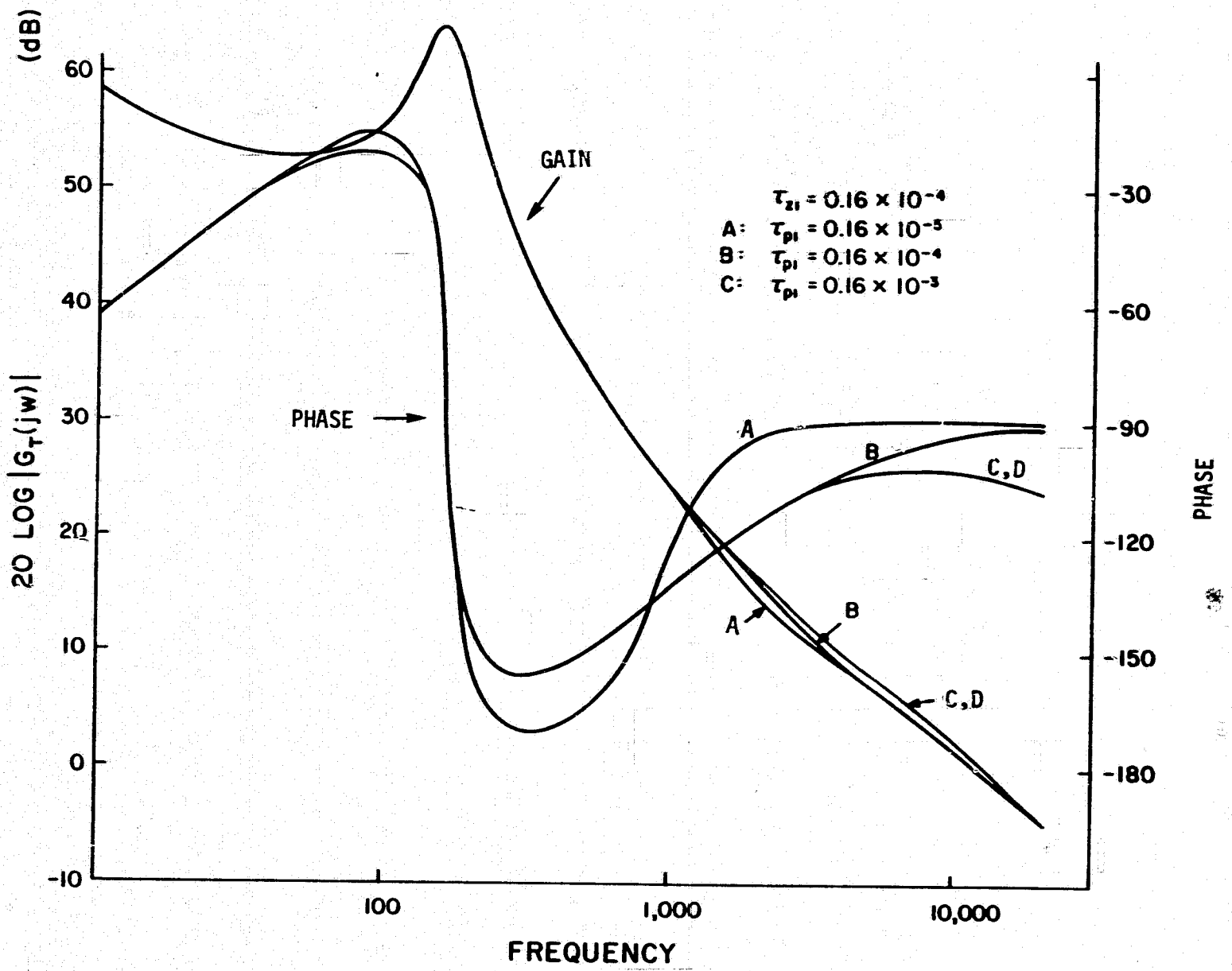


Fig. 5.2. Open loop characteristics for a fixed τ_{z1} and three τ_{p1} values

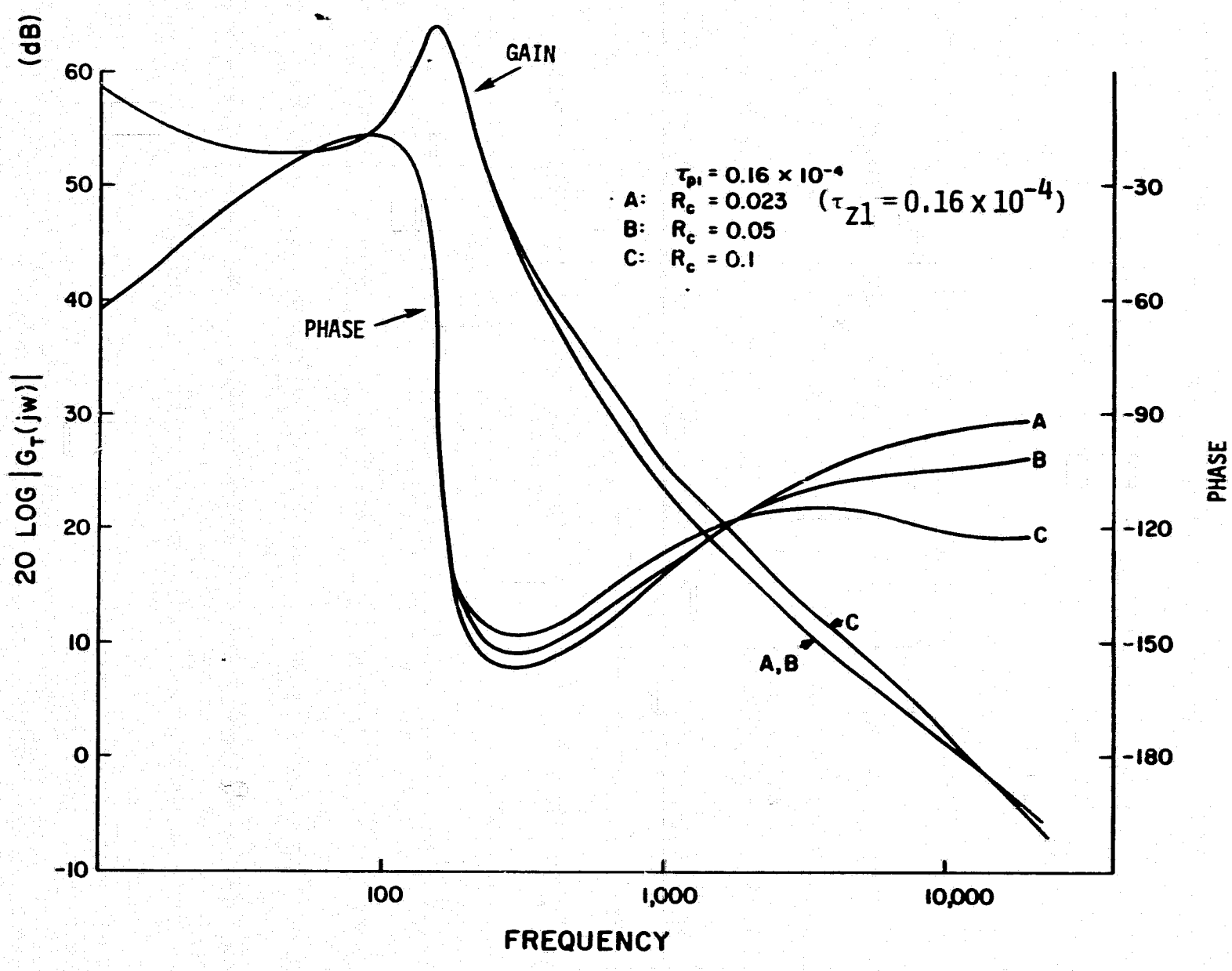


Fig. 5.3. Open-loop characteristics for a fixed τ_{p1} and three τ_{z1} values.

Examining Fig. 5.2, it appears that a large τ_{p1} (curve A) is preferable to a smaller τ_{p1} (curves C and D). This is not necessarily the case, however, if one examines the audiosusceptibility characteristic or the output impedance characteristic. The output impedance characteristic of a buck/boost converter employing three τ_{p1} values is shown in Fig. 5.4. For larger τ_{p1} (curve A), an apparent increase of the output impedance is shown at the corner frequency $1/(2\pi\tau_{p1})$. A similar characteristic can also be observed for the converter audiosusceptibility. A qualitative explanation is that the inclusion of the $\tau_{p1}s + 1$ term when $\tau_{p1} \neq \tau_{Z1}$ introduces an additional pole s_{04} to the output impedance transfer function as shown in Fig. 5.5. When the magnitude of τ_{p1} is increased, the pole s_{04} is moved to the right and merged to the pole s_{01} to form a complex pair which results in the peaking effect shown in Fig. 5.4.

From the above discussion it is quite obvious that an adverse effect will inevitabley occur when the equality constraint (5.1) is violated. A deliberate measurement of the output filter ERS is therefore in order. It should be noted, however, that the equality constraint (5.1) is introduced mainly to simplify the mathematical expression of the open-loop characteristic. When such an equality constraint is not easily achievable in a practical design, one could consider using a small τ_{p1} value such that it will not introduce any significant phase delay in the frequency range of interest. Employing Fig. 5.2 for example, a τ_{p1} value of 0.16×10^{-5} or 0.16×10^{-6} should be chosen to avoid any adverse effect.

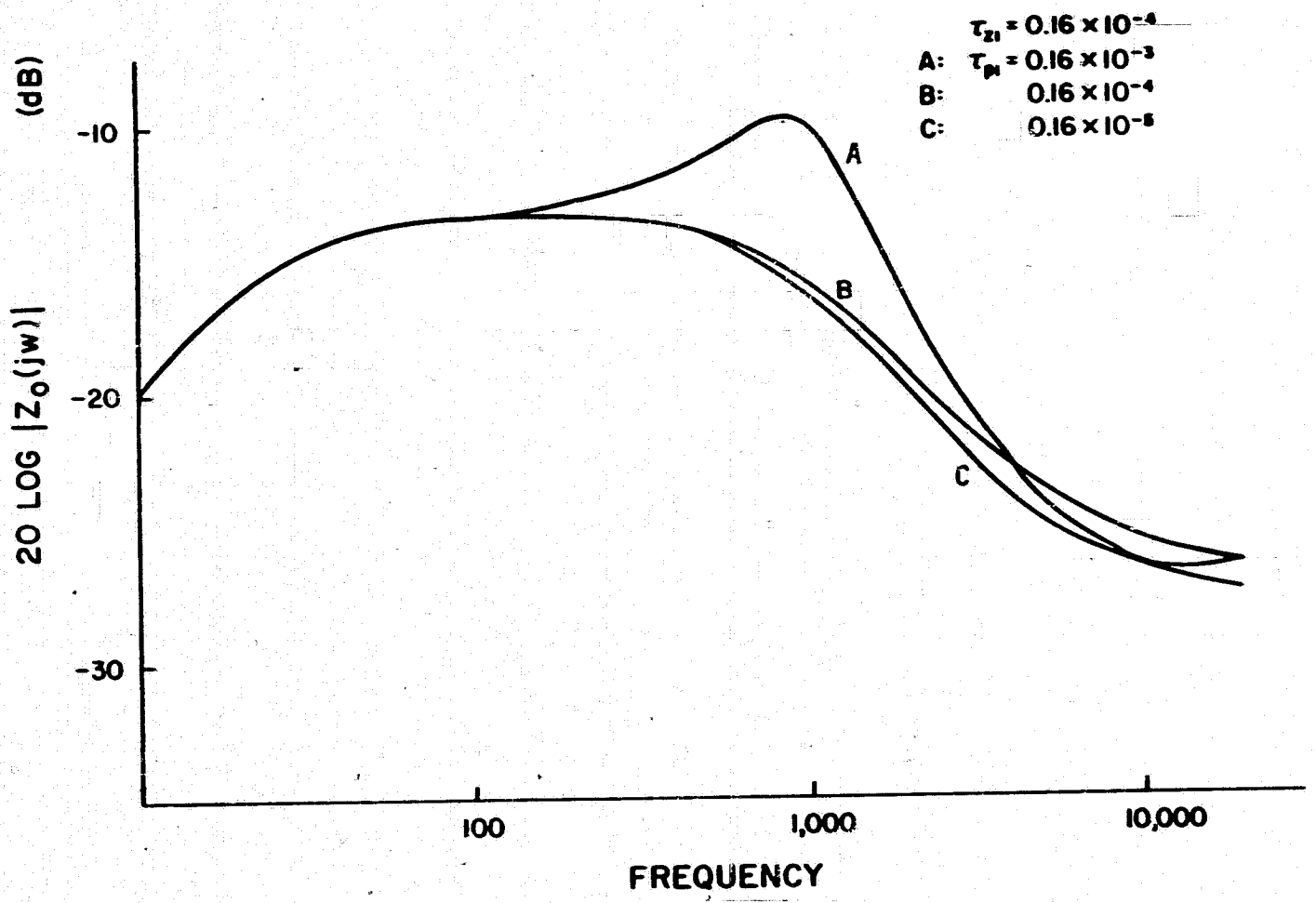


Fig. 5.4. Output impedance characteristics for three τ_{p1} values

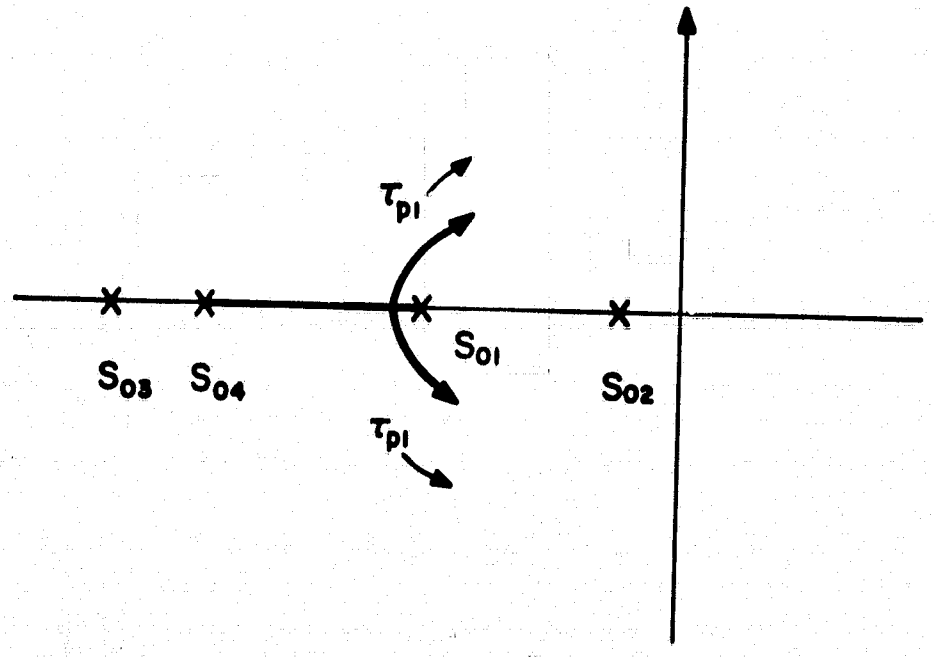


FIG. 5.5 CHARACTERISTIC ROOTS OF THE CLOSED LOOP REGULATOR

(2) The roots of the open-loop-characteristic second-order-zero are assumed to be real and sufficiently apart so that the following approximation is valid:

$$\frac{1}{\alpha'} s^2 + \tau'_{Z2}\omega_o s + 1 = \left(\frac{s}{s_{o1}} + 1\right)\left(\frac{s}{2_{o2}} + 1\right) \qquad (5.2)$$

where $s_{o1} \tilde{=} \alpha'\omega_o\tau'_{Z2}$

$$s_{o2} \tilde{=} \frac{1}{\omega_o\tau'_{Z2}}$$

(3) The open loop gain is assumed sufficiently large so that the audio-susceptibility $G_A(s)$ and the output impedance $Z_o(s)$ can be approximated by (3.28) and (3.37), respectively. The approximation simplifies the high frequency characteristic by ignoring a high-frequency pole, but makes no simplification of the low frequency characteristic. This assumption is valid since the worst case audio-susceptibility and output impedance usually occur at low frequencies so that only the simplified equations (3.28) and (3.37) are of design importance.

(4) Complications due to the high frequency pole and described in Volume I can be avoided by observing the following assumption:

$$s_{o1} < 1/(\omega_o\tau_{Z1}) \qquad (5.3)$$

If the above inequality is satisfied, the maximum $G_A(s)$ or $Z_o(s)$ will occur at a frequency between s_{o1} and s_{o2}. Based on assumptions 2 and 4, s_{o1} and s_{o2} are confined to a certain frequency range as shown in Fig. 5.6.

(5) The magnitude of τ_{Z2} is assumed sufficiently large so that the following approximation holds:

$$\tau'_{Z2} = \tau_{Z2} \tag{5.4}$$

While this assumption is true for all practical designs, it is not a necessary one in the design procedure to follow.

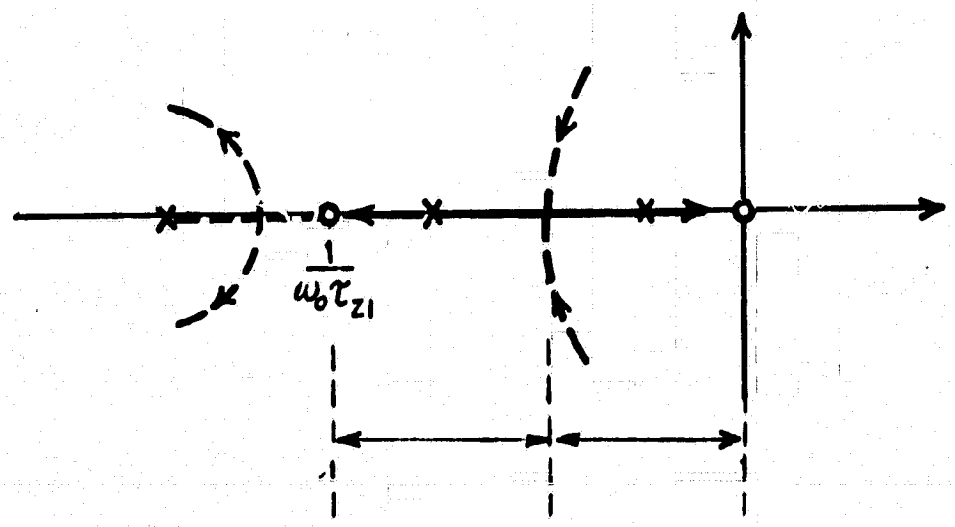
(6) Input filter effect on the stability and output impedance characteristics may be neglected if the following relation is observed:

$$B_R = Z_F(j\omega_1) << \mu^2 R_L. \tag{5.5}$$

As a rule of thumb, the peaking B_R should be less than 20 percent of $\mu^2 R_L$ which is rather a relaxed constraint for input filter design. Usually, the audiosusceptibility requirement will impose a tighter constraint on B_F as well as on B_R.

5.4 Design Constraints.

(1) Audiosusceptibility requirement. The switching regulator performance specifications are presented in the form of design constraints. In converter design, the maximum tolerable magnitude of $|G_A(s)|$ is normally specified as K_A. Employing eq. (3.29) without an input filter, one obtains



$$\frac{1}{\omega_o \tau_{z1}} > |s_{o1}| > 1 \quad , \quad 1 > |s_{o2}| > 0$$

FIG. 5.6 DESIGN RANGES FOR THE ZEROS S_{o1} AND S_{o2} FOR BETTER REGULATOR PERFORMANCE

c-2

$$20 \log |G_A(s)|_{max} = 20 \log \left(\frac{K_2}{K_1} \frac{1}{\alpha \tau'_{z2}}\right) \leq 20 \log K_A \qquad (5.6)$$

Employing eq. (4.11) with an input filter, one obtains

$$20 \log |G_A(s)|_{max} = 20 \log \left(\frac{K_2}{K_1} \frac{1}{\alpha \tau'_{z2}}\right) + 20 \log \frac{B_F}{1-B_R/(\mu^2 R_L)}$$

$$\leq 20 \log K_A \qquad (5.7)$$

Eq. (5.7) is derived with the assumption that the input filter resonant frequency occurs between $|s_{o2}|$ and $|s_{o1}|$ (which is generally the case). Thus:

$$S_{o2} < \frac{\omega_1}{\omega_o} < S_{o1} \, . \qquad (5.8)$$

If (5.8) is not satisfied, the effect of input filter peaking on the audiosusceptibility performance is less profound than indicated in (5.7).

The minimum audiosusceptibility that can be achieved by any control circuit design for a given power stage was derived in (3.32) as

$$\min\{|G_A(s)|_{max}\} = \frac{K_2}{K_1} \frac{R_C}{L_e} \frac{\alpha'}{\alpha} \qquad (5.9)$$

Taking logarithms as before,

$$20 \log \left[\min \{ |G_A(s)| \max \}\right] = 20 \log \left(\frac{K_2}{K_1} \frac{R_c}{L_e} \frac{\alpha'}{\alpha'} \right) \qquad (5.9a)$$

Thus, $20 \log |G_A(s)|$ must satisfy the inequality

$$20 \log \left(\frac{K_2}{K_1} \frac{R_c}{L_e} \frac{a'}{a}\right) \leq 20 \log |G_A(s)| \leq 20 \log \left(\frac{K_2}{K_1} \frac{1}{\alpha \tau'_{z2}}\right) + 20 \log \frac{B_F}{1-B_R/\mu^2 R_L} \leq 20 \log K_A$$

(5.9b)

(2) Output impedance requirement. A maximum output impedance should be specified as K_o. Employing eq. (3.38), one obtains

$$\left| Z_o(s) \right|_{max} = \frac{L_e}{\alpha \tau'_{Z2}} = K_o \tag{5.10}$$

The best achieveable output impedance for a given power stage design was derived in (3.39) as

$$\min \left\{ \left| Z_o(s) \right|_{max} \right\} = R_C \frac{\alpha'}{\alpha} \tag{5.11}$$

(3) Stability requirement. It is a presumption in any switching regulator design that the circuit should provide stable operation under all line conditions, load conditions, and environmental changes. The assurance of a stable operation is usually provided only after the circuit has undergone a series of rigorous tests. The objective here is not in an attempt to eliminate the necessity of such a test procedure, but rather to add an additional degree of confidence in the design stage. To achieve this, one can specify the open loop crossover frequency and the phase margin. The former assures a high-gain, wide-bandwidth loop characteristic, and the latter assures a stable operation.

(4) Transient response requirements due to a step load change. In section 3.6, it was discussed that if $s'_{o1} >> s'_{o2}$, then the time constant $1/s'_{o2}$ determines the decay rate of the transient response due to a step change of load current.

For convenience, the symbol τ_s is used to represent the time constant $1/s'_{o2}$:

$$\tau_s = 1/s'_{o2} \tag{5.12}$$

It should be noted that when the SCM design guidelines are followed, transient response is always in the form of exponential decay without oscillation.

The amount of peaking due to load changes can be limited through the design of the control loops. In the design specification, the maximum peaking voltage is expressed as a percentage ($K_{OP}\%$) of the nominal dc output voltage. Referring to (3.46) one obtains

$$\left(\frac{\Delta V_{o\ max}}{V_o}\right)/\left(\frac{\Delta I_o}{I_o}\right) = \frac{|Z_{o\ max}|}{R_L} \leq K_{op} \tag{5.13}$$

It is important to note that there exists a theoretical limit on the lower bound of $|Z_{o\ max}|$ given in (5.11). The transient response K_{op} can not be specified at a value less than $\frac{R_C}{R_L}\frac{\alpha'}{\alpha}$ since this requirement can not be realized in any SCM design.

(5) DC Regulation. The percentage change K_{DC} of the output voltage with respect to its nominal value due to the line voltage variation is derived in (3.52)

$$\left(\frac{\Delta V_o}{V_o}\right)/\left(\frac{\Delta V_I}{V_I}\right) = \left(F_M K \frac{gR_4}{R_4+R_x}\right)^{-1} \frac{F_I(o)}{F_D(o)} \frac{V_I}{V_o} \leq K_{DC} \tag{5.14}$$

where K is the dc gain of the operational amplifier and $F_I(o)$ and $F_D(o)$ are specified in (3.51).

(6) Other design constraints. In practical design, the voltage swing at the output of the operational amplifier integrator shown in Fig. 5.7 should be confined to a permissible operating voltage range (V_{T1}, V_{T2}). For example, if the LM101 chip is used with a 5-volt supply, the safe operating range may be defined as

$$V_{T1} \geq 2 \text{ Volts}$$

$$V_{T2} \leq 4 \text{ Volts}$$

Once V_{T1} and V_{T2} have been selected, the proper ac-loop time constant may be determined. It is useful to define two terms, S_N and S_F, where:

S_N is the absolute value of the slope of $V_T(t)$ during T_{on}, and

S_F is the absolute value of the slope of $V_T(t)$ during T_{off}.

With these definitions in hand, the following criterion may be set:

$$S_N T_{on} = S_F T_{off} < V_{T2} - V_{T1} \qquad (5.15)$$

For the buck converter, $S_N = n\,(V_I - V_o)/R_4C_1$ and $T_{on} = V_o T_p / V_I$. Substitution of these expressions into equation (5.15) yields an expression for the ac-loop time constant:

$$R_4C_1 > \frac{nV_o(1-D)T_p}{V_{T2}-V_{T1}} \qquad (5.16)$$

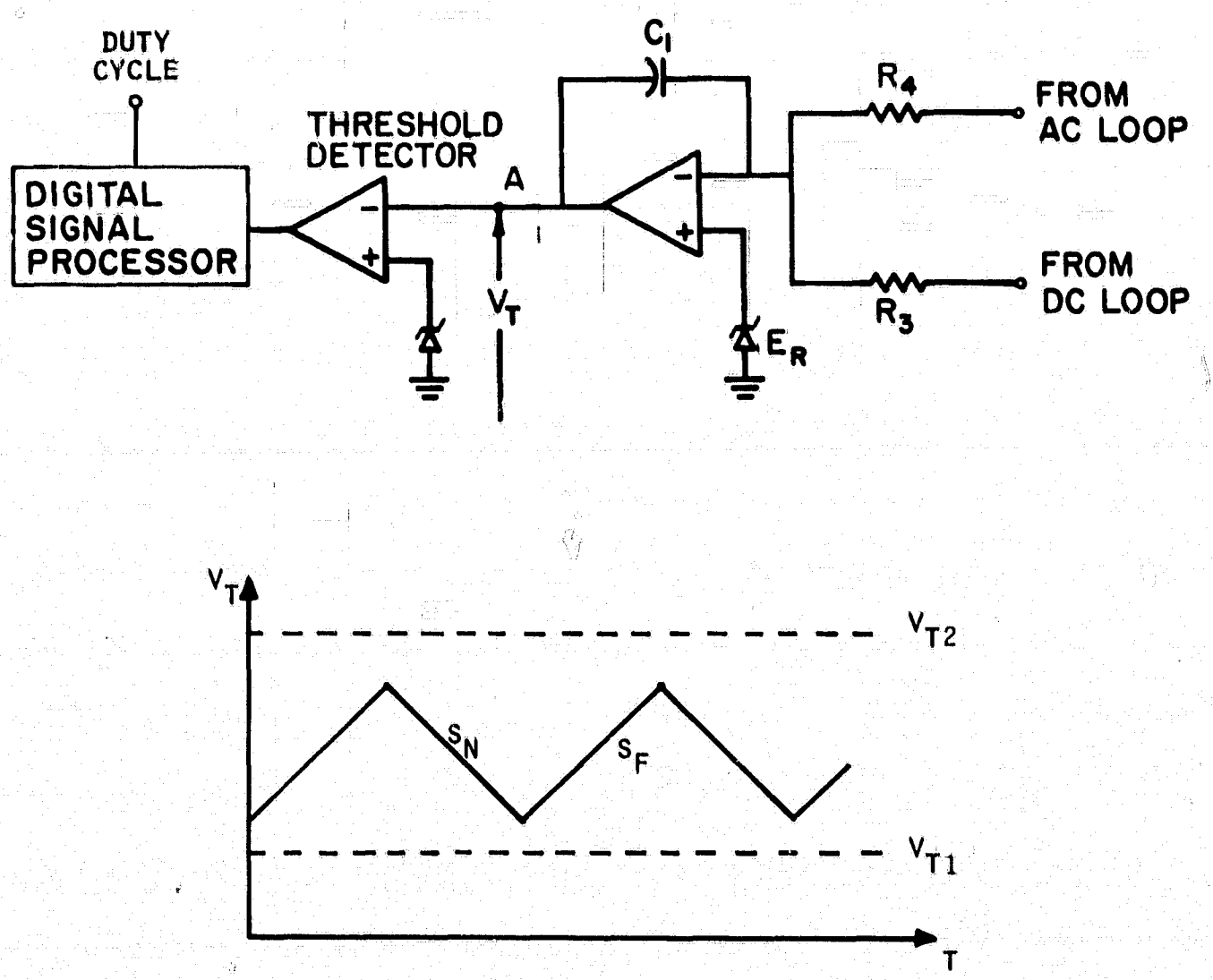


FIG. 5.7 PRACTICAL LIMITS FOR THE INTEGRATOR OUTPUT VOLTAGE

Similarly for the boost and buck/boost converters:

$$R_4C_1 > \frac{nV_oDD'T_p}{V_{T2}-V_{T1}} \qquad \text{boost} \qquad (5.17)$$

$$R_4C_1 > \frac{nV_oD'T_p}{V_{T2}-V_{T1}} \qquad \text{buck/boost} \qquad (5.18)$$

5.5 Design Trade-Offs.

Since the number of design variables is usually greater than the number of design equations, there exists a potentially infinite set of designs that satisfy the given design constraints. Among this infinite set of "acceptable" designs, however, a particular design might be identified which would optimize certain performance characteristics deemed more desireable than others. The process of obtaining this optimum design naturally involves design trade-offs of one performance characteristic for another. Since the performance characteristic to be optimized varies from one design case to another, only a general basis for design trade-off and optimization will be provided. Precautions to be applied in setting up the optimization strategies are given.

(1) The inaccuracies of the switching regulator model at high frequencies.

The accuracy of the power stage model, which is derived using the State Space Averaging technique, degenerates as the modulation frequency approaches half the switching frequency especially in predicting phase delay. The simplified pulse modulator model, derived using the describing functional technique, also becomes inaccurate at high frequencies. This model disregards the phase delay entirely. Experimental measurements of pulse modulator gain and

phase are shown in Figures 7.8 and 7.9 of Volume I. While the model inadequacies may be neglected in the single-loop system, they cannot be neglected in the multiple-loop SCM system being considered here. SCM control provides high open-loop cross-over frequency. Precautions must be taken in examining the phase margin since the model does not provide accurate phase delay information in this high frequency range. Adequate stability margin can be determined only when the model deficiencies are fully understood and taken into account.

(2) Trade-off between stability and other regulator performance.

As discussed in section 3.6, the settling time of the load transient response in dominated by the zero s_{o2} of the open loop transfer function. It is shown in Fig. 5.8 that the variation of s_{o2} with s_{o1} kept constant, affects the open-loop characteristic in the low frequency range. To provide sufficient phase margin throughout the frequency spectrum of practical concern, the corner frequency at s_{o2} should be sufficiently smaller that the output filter resonant frequency ω_o. Why this is so is seen by considering the extreme case when $s_{o2} \rightarrow \infty$. In this case, the open loop phase delay approaches -270^o for frequencies greater than the filter resonant frequency. Therefore the trade-off between stability and transient response should be considered.

The open-loop gain can be increased effectively by changing s_{o1} while selecting an optimum value for s_{o2}. These changes can be achieve by simply varying the parameter α'. To achieve a higher gain, wider bandwidth open-loop characteristic requires the use of larger α'.

Increasing α', however, increases the phase delay, as illustrated in Fig. 3.3. This increased phase delay is undesirable from the stability point of view. Since the crossover frequency is usually high (approximately 1/3 or 1/2 of the switching frequency), and since the additional phase delay due to the pulse modulator, the transport lag, and the inaccuracy of the power stage model cannot be accurately accounted for in the analytical model, a phase margin of 70° or 80° should be provided, when possible, to ensure stable operation.

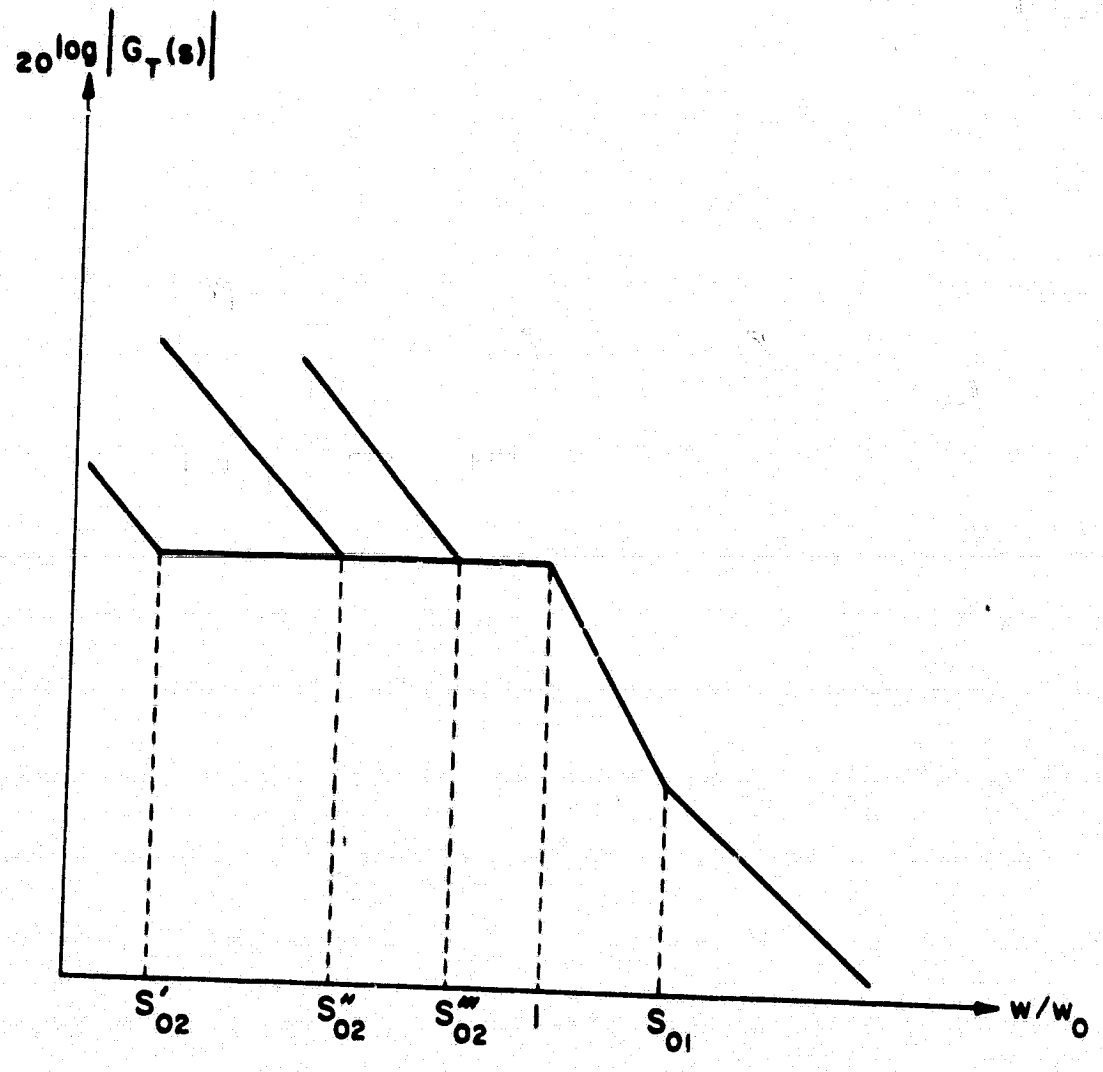


FIG. 5.8 OPEN LOOP TRANSFER CHARACTERISTIC FOR DIFFERENT VALUES OF THE ZERO S_{02}

CHAPTER VI

DESIGN PROCEDURES AND EXAMPLES

6.1 Design Procedures.

Based on the design assumptions and design constraints specified in Chapter V, key control circuit parameters can be derived according to the following design procedures.

Step 1: Employing the settling time of the output transient response of (5.12), one can determine the range for s_{o2}

$$s_{o2} \geq \frac{1}{\omega_o \tau_s} \qquad \text{or} \qquad \tau'_{z2} \leq \tau_s \tag{6.1}$$

where τ_s defines the upper limit of τ'_{z2} according to the specified characteristic requirement.

Step 2: The peaking constraint due to a step load change shown in eq. (5.13) is used to compute a lower bound, M_1, of s_{o1}.

$$s_{o1} \geq \frac{\frac{\omega_o L_e}{A_1 R_L}}{K_{op} - \frac{A_2 L_e}{A_1 R_L}} \triangleq M_1 \tag{6.2}$$

$$K_{op} \triangleq \left(\frac{\Delta V_{o\ max}}{V_o} \right) / \left(\frac{\Delta I_o}{I_o} \right) \tag{6.3}$$

K_{op} is defined to be the worst tolerable transient peaking.

Step 3: The audiosusceptibility constraint (5.6) or (5.7) is used to determine additional lower bounds, M_2 and M_3, of s_{o1}.

(A) Without an input filter:

$$s_{o1} \geq \frac{\frac{K_2}{K_1}\frac{\omega_o}{A_1}}{K_A - \frac{K_2}{K_1}\frac{A_2}{A_1}} \triangleq M_2 \tag{6.4}$$

where 20 log K_A is defined as the worst tolerable audiosusceptibility.

(B) With an input filter:

$$s_{o1} \geq \left(\frac{K_2}{K_1}\frac{\omega_o}{A_1}\right)/\left(K'_A - \frac{K_2}{K_1}\frac{A_2}{A_1}\right) \triangleq M_3 \tag{6.5}$$

$$\text{where } K'_A = K_A\left(1 - \frac{B_R}{\mu^2 R_L}\right)/B_F \tag{6.6}$$

Step 4: The output impedance constraint (5.10) is used to compute a lower bound, M_4, of s_{o1}.

$$s_{o1} \geq \left(\frac{\omega_o L_e}{A_1}\right)/\left(K_o - L_e\frac{A_2}{A_1}\right) \triangleq M_4 \tag{6.7}$$

Step 5: The upper bound of s_{o1} is determined by (5.3)

$$s_{o1} \leq \sqrt{\frac{L_e}{C}}\ \frac{1}{R_c} \triangleq B_2 \tag{6.8}$$

Step 6: The feasible range for s_{ol} is determined by using the results obtained in step 2 through step 5.

$$B_1 \leq s_{ol} \leq B_2 \tag{6.9}$$

where $B_2 = \sqrt{\frac{L_e}{C}} \frac{1}{R_c}$

and $B_1 \triangleq \text{MAX}\ \{M_1, M_2(\text{or } M_3), M_4\}$

It should be noted chat a feasible value for s_{ol} may not be attainable from the inequality constraint eq. (6.9) implying that either the constraints are not specified properly or they are not achievable by any control loop design with the given power stage parameters. (Refer to discussion in section 5.4 concerning some theoretical limits on regulator performances). Under this condition the design specifications must be relaxed, or else the power stage parameters must be redesigned to accommodate the specification. For example, the worst audiosusceptibility is specified in the design constraint (5.6):

$$|G_A(s)|_{max} \leq K_A$$

If K_A is greater than the practical limit shown in (5.9), a feasible value for s_{ol} can never be obtained. Similarly, if K_o is greater than the practical limit of $|Z_o(s)|_{max}$ in (5.11), the design can never be realized.

Step 7: The open loop characteristic is now used to establish stability criteria. These criteria, in conjuntion with the previously derived feasible ranges for s_{o1} and s_{o2} in (6.1) and (6.9), establish the backbone of the design guidelines. Since $s_{o1} = \omega_o \alpha' \tau'_{z2}$ and $s_{o2} = 1/(\omega_o \tau'_{z2})$, the feasible ranges for τ'_{z2} and α' can be determined. Proper values for τ'_{z2} and α' can be selected from a given set of open loop gain and phase curves provided in the Appendix. These curves are constructed for different values of $\omega_o \tau'_{z2}$ ranging from 1 to 10 and α'=(0.04, 0.1, 0.2, 0.4, 0.6, 0.8, 1.0, 2, 3, 4, 5, and 6). It should be noted that the damping constant $\zeta = 0.2$ is employed for these gain and phase plots. The effect of different damping constant ζ is illustrated and is shown to be significant only within a decade from the natural frequency ω_o. Since the crossover frequency is generally more than a decade from the natural frequency ω_o, different damping constant imposes negligible effect in determining the crossover frequency and phase margin of the system. The value of τ'_{z2} is first chosen with the help of (6.1). Having chosen τ'_{z2}, the corresponding open-loop characteristics may be used to select the best α' such that adequate stability margin is provided and all design constraints are satisfied concurrently. It should be noted that the vertical scale of the open loop characteristics in the Appendix are normalized by a factor (k_1/ω_o) (α/α') so that these curves can be applied to all three switching regulator types.

Step 8: From *Step* 1 and *Step* 7 the values for α' and τ'_{z2} can be determined. Once α' and τ'_{z2} are defined, the calculation of all control circuit parameters, namely R_1, R_2, R_3, R_4, R_5, C_1, C2, and n becomes a straightforward task.

6.2 Design Examples

Four design examples are given to demonstrate the design procedures described in the previous section. They are:

Example 1. Design a SCM control circuit for a buck converter without an input filter. For simplicity, consider a fixed input voltage and output power.

Example 2. Same as example 1 design, except that a two-stage input filter is employed.

Example 3. Similar to example 1 design, except that an input voltage range and an output power range are considered.

Example 4. Design the SCM control circuit for a buck/boost converter at a condition similar to that of Example 1.

Example 1. Design the SCM control circuit for the buck converter shown in Fig. 1.1. For simplicity, consider first a fixed input voltage, without an input filter, and a predetermined duty cycle control mode (constant $V_I T_{ON}$ control).

Input - output requirements.

V_I = 50 volts

V_0 = 20 volts

D = 0.4

P_0 = 40 watts.

Power stage parameters.

L = 230 μH

C = 300 μF

R_ℓ = 0.2 ohm

R_C = 0.067 ohm (nominal)

R_L = 10 ohms

Pulse modulator parameters.

T_{ON} = 17.6 μsec.

$M = V_I T_{ON} = 0.88 \times 10^{-3}$ V-sec.

Other key power stage parameters can be calculated.

$\omega_0 = 3.807 \times 10^3$ rad/sec.

ζ = 0.158

$\mu = 1/D = 2.5$

$K_1 = 1.136 \times 10^5$

$K_2 = D = 0.4$

$\left.\begin{matrix} A_2 = 0 \\ A_1 = 1 \end{matrix}\right\}, \alpha = \alpha'$

The design specifications are given as follows.

(1) The audiosusceptibility should be less than -35 db for all frequencies, i.e. $K_A = 0.01778$.

(2) The output impedance should be less than 0.5 ohm for all frequencies, i.e. $K_0 = 0.5$.

(3) The phase margin at the crossover frequency should be greater than 70°.

(4) Load transient response:

(a) Time constant, $\tau_s < 2$ msec.

(b) Output voltage peaking should be less than 0.5% of the nominal dc value for a 10% step change of the output current from its nominal value, i.e. $K_{OP} = 0.05$.

(5) DC regulation

$$\left(\frac{\Delta V_o}{V_o}\right) / \left(\frac{\Delta V_I}{V_I}\right) \leq K_{DC} = 10^{-6}$$

Design procedures:

Step 1:

The time constant of the transinent is determined from (6.1):

$$\tau'_{z2} \leq 2 \times 10^{-3} \text{ sec.}$$

or $s_{o2} \geq 0.131$

Step 2:

Step load transient response constraints is determined from (6.2) and (6.3):

$$s_{ol} \geq M_1 \triangleq \frac{\omega_0 L/R_L}{K_{OP}} = 1.751$$

Step 3:

Audiosusceptibility constraint is determined from (6.4):

$$s_{ol} \geq M_2 \triangleq \frac{\omega_0 K_2/K_1}{K_A} = 0.754$$

Step 4:

Output impedance constraint is determined from (6.7):

$$s_{o1} \geq M_4 \triangleq \frac{\omega_0 L}{K_0} = 1.751$$

Step 5:

The upper bound of s_{o1} is determined from (6.8):

$$s_{o1} \leq \frac{1}{\omega_0 \tau_{z1}} = 13$$

Step 6:

The feasible ranges for s_{o1} and s_{o2} are determined from (6.9):

$$B_1 = \text{Max}\{M_1, M_2, M_4\} \leq S_{01} \leq B_2 = 13$$

$$1.751 \leq s_{o1} \leq 13$$

$$0.131 \leq s_{o2}$$

The feasible range of the product $\alpha'\tau'_{z2}$ can now be determined using the relationship $s_{o1}/\omega_o = \alpha'\tau'_{z2}$ in conjunction with the feasible range for s_{o1} found in *Step 6:*

$$4.6 \times 10^{-4} \leq \alpha'\tau'_{z2} \leq 3.43 \times 10^{-3}$$

Step 7:

If we choose $\tau'_{z2} = 1.31 \times 10^{-3}$ sec., then $\omega_o\tau'_{z2} = 5$. Using this value of τ'_{z2}, the feasible range for α' may be determined from the result of *Step 6:* $0.35 \leq \alpha' \leq 2.62$. Curves of gain and phase corresponding to this feasible range are shown darkened in Fig. 6.1, the set of open-loop characteristics corresponding to $\omega_o\tau'_{z2} = 5$. (These curves are given again in Fig. A.6).

The phase margin requirement is considered next. Since the vertical scale of the open-loop gain characteristic is normalized by the factor $(K_1\alpha)/(\omega_o\alpha')$, a magnitude of $20 \log \left(\frac{K_1\alpha}{\omega_o\alpha'}\right)$ should be added to Fig. 6.1(a) to represent the actual open-loop gain. Since $\alpha = \alpha'$ in this example, we have

$$20 \log (K_1/\omega_0) = 29.5 \text{ db.}$$

From Fig. 6.1, one can find that the crossover frequency $f_x \approx 33\ f_0$ for the entire feasible range of α'. The phase margins are found from Fig. 6.1(b):

For $\alpha' = 2.62$, phase margin = 60°
For $\alpha' = 0.35$, phase margin = 85°

It is shown that the larger magnitudes of α' within the feasible range fail to provide the phase margin minimum of 70° specified in the design requirement. Therefore, a compromise between performance optimization, which requires a larger α', and system stability margin, which demands smaller α', has to be made. It should be noted that a minimum of 70° phase margin which is specified in the design requirement is employed merely to provide a comfortable design margin to take into account the model inaccuracies. Failure to satisfy this particular constraint does not imply system instability. It is the user's discretion at this design stage either to select the largest possible α' for best achievable performance characteristics or to select the smallest possible α' to merely satisfy the performance specification while offering the largest possible stability margin.

Step 8:

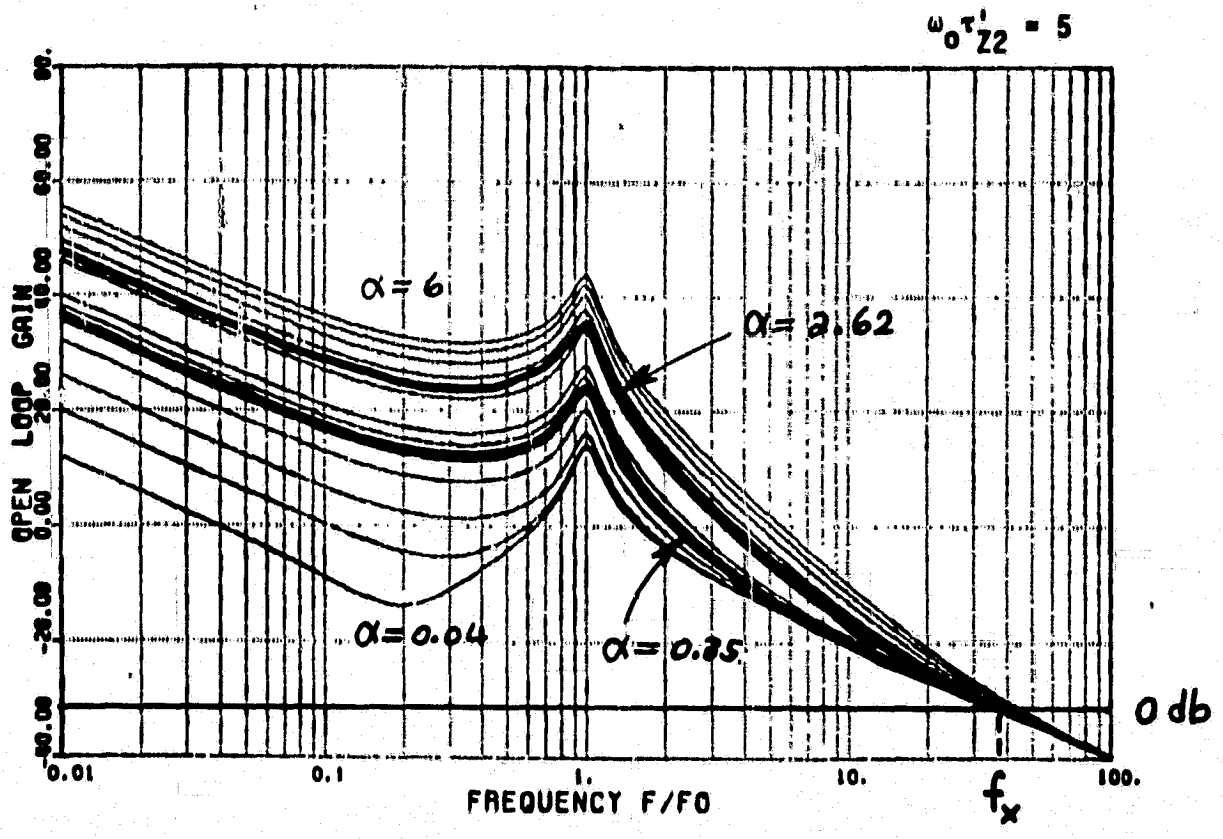
Determine the control circuit parameters R_1, R_2, R_3, R_4, R_5, C_1, C_2, and n. Since the number of unknowns is greater than the number of equations, the following parameter values are selected arbitrarily:

$E_R = 6.7$ V

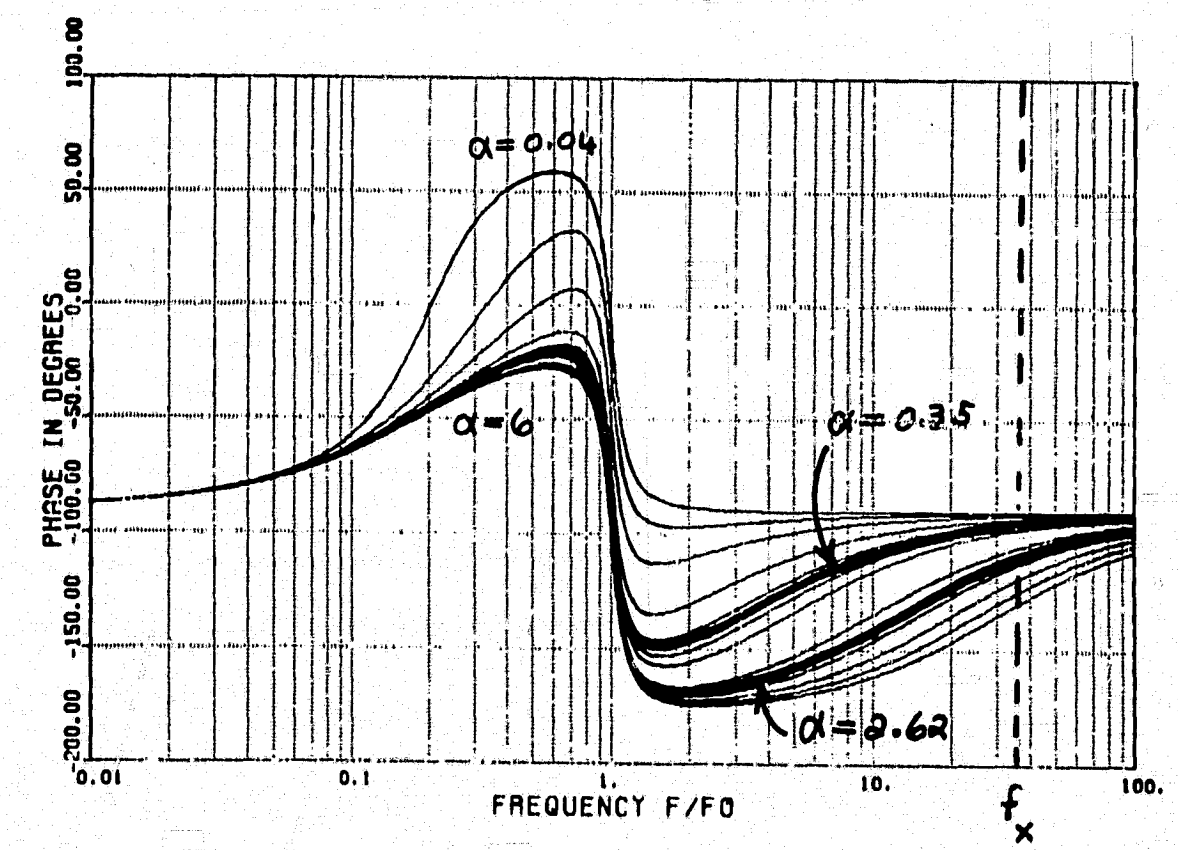
$R_1 = 33.3$ KΩ

$R_2 = 16.7$ KΩ

$n = 0.65$



a) OPEN-LOOP GAIN



b) OPEN-LOOP PHASE

FIG. 6.1 OPEN-LOOP CHARACTERISTICS FOR A BUCK CONVERTER WITH $\omega_o\tau'_{Z2} = 5$

To provide a good stability margin, $\alpha(=\alpha')$ is chosen to be 0.355. This choice gives:

$$R_4/R_x = 0.692 \qquad (A)$$

From (5.1), $R_5C_2 = R_CC = 2 \times 10^{-5}$ (B)

From *Step 7*, $\tau'_{z2} = 1.76 \times 10^{-3}$

$$(R_5 + \frac{R_x+R_3}{g})C_2 \simeq \frac{R_x+R_3}{g} C_2 = 1.76 \times 10^{-3}$$

$$(R_x+R_3)C_2 = 5.86 \times 10^{-4} \qquad (C)$$

From (5.16) for $V_{T2} = 4$, $V_{T1} = 2$

$$R_4C_1 > 1.7.6 \times 10^{-4} \qquad (D)$$

From (5.14)

$$R_4C_1\frac{R_4}{R_4 + R_x} \geq \frac{1}{2} \frac{M}{Kg} \frac{F_I(0)}{F_D(0)} \frac{1}{K_{DC}}$$

$$R_4C_1\frac{R_4}{R_4 + R_x} \geq 6.87 \times 10^{-5} \quad \text{(using } K = 10^5\text{)} \qquad (E)$$

The above five equations (A) to (E) can be used to solve for the five unknowns, R_4, R_3, R_5, C_1 and C_2.

$R_4 = 40.7\ K\Omega$

$R_3 = 47\ K\Omega$

$R_5 = 2000\ \Omega$

$C_1 = 5600$ pf

$C_2 = 0.01\ \mu f.$

A test circuit was built using these parameter values. Test results are summarized in Table 6.1. Figures 6.2 to 6.5 present the theoretical and measured results of switching regulator performance characteristics with excellent correlations. It should be noted that a measured phase margin of 50° is reported rather than the theoretically predicted phase margin of 85°. This discrepancy is due to the inaccuracies of the power stage and pulse modulator models at high frequencies discussed earlier.

TABLE 6.1 SUMMARIES OF THE BUCK REGULATOR PERFORMANCE CHARACTERISTICS

	THEORY	MEASUREMENT	SPECIFICATIONS
CROSSOVER FREQUENCY (HZ)	14000	12000	N/A
PHASE MARGIN	85^0	50^0	70^0
AUDIO-SUSCEPTIBILITY (DB)	-45	-43.5	-35
OUTPUT IMPEDANCE (OHM)	0.375	0.407	0.5
TRANSIENT SETTLING TIME	1.76	1.8	2
TRANSIENT PEAKING $\frac{\Delta V_0}{V_0} / \frac{\Delta I_0}{I_0}$	0.038	0.03	0.05

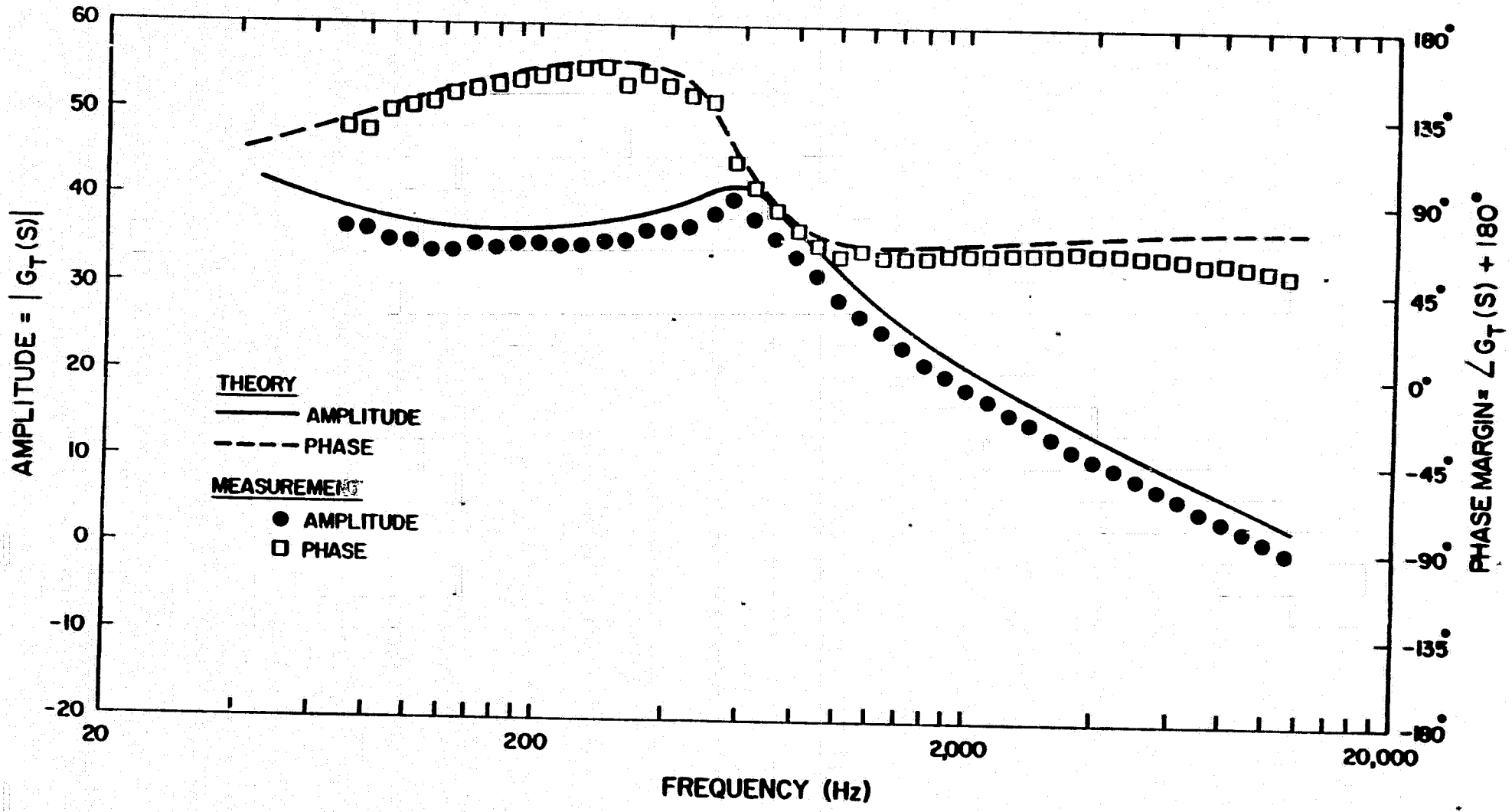


FIG. 6.2 OPEN LOOP GAIN AND PHASE OF THE BUCK CONVERTER IN *Example 1* DESIGN

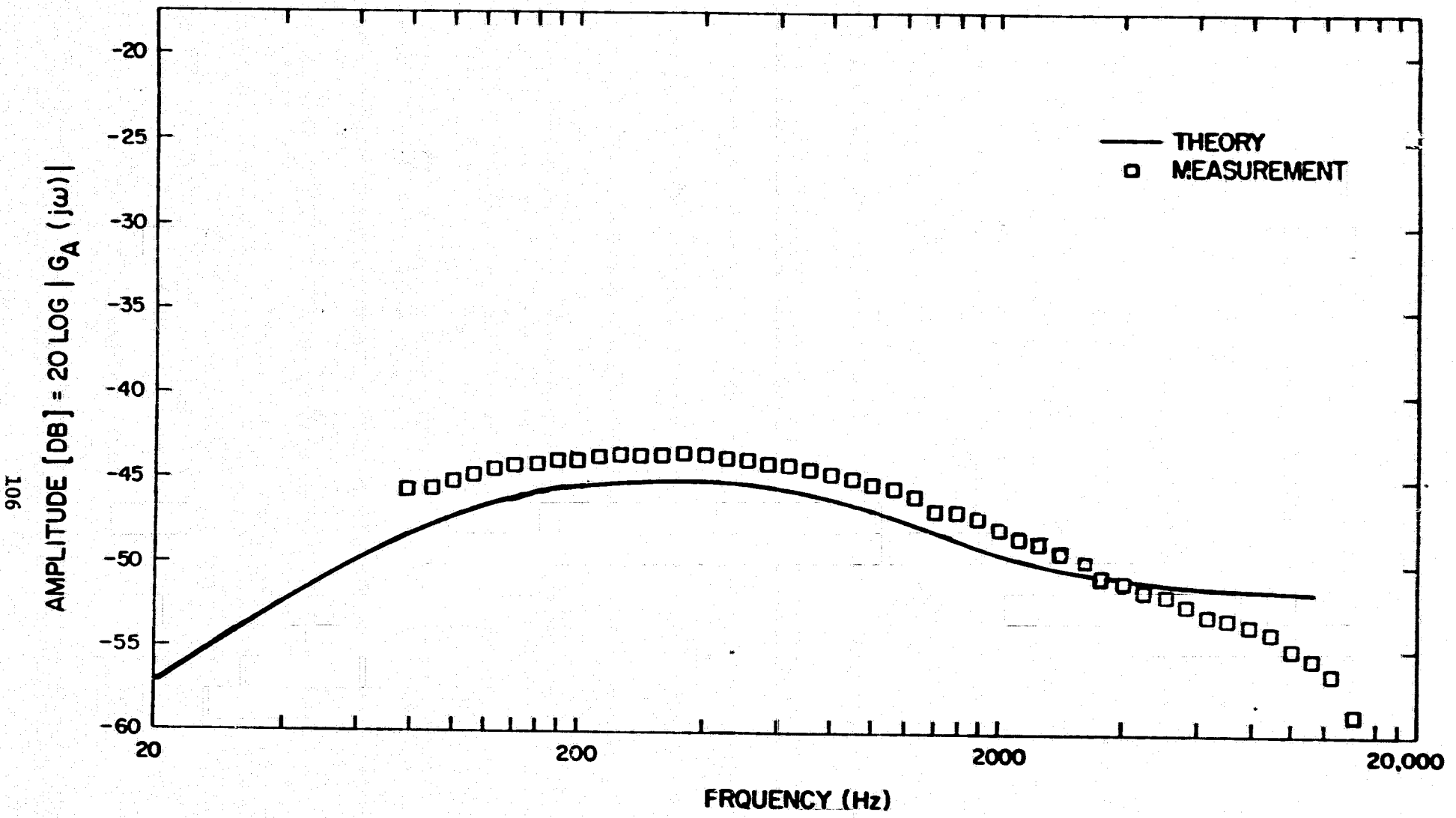


FIG. 6.3 AUDIOSUSCEPTIBILITY CHARACTERISTIC OF THE BUCK CONVERTER IN *Example 1* DESIGN

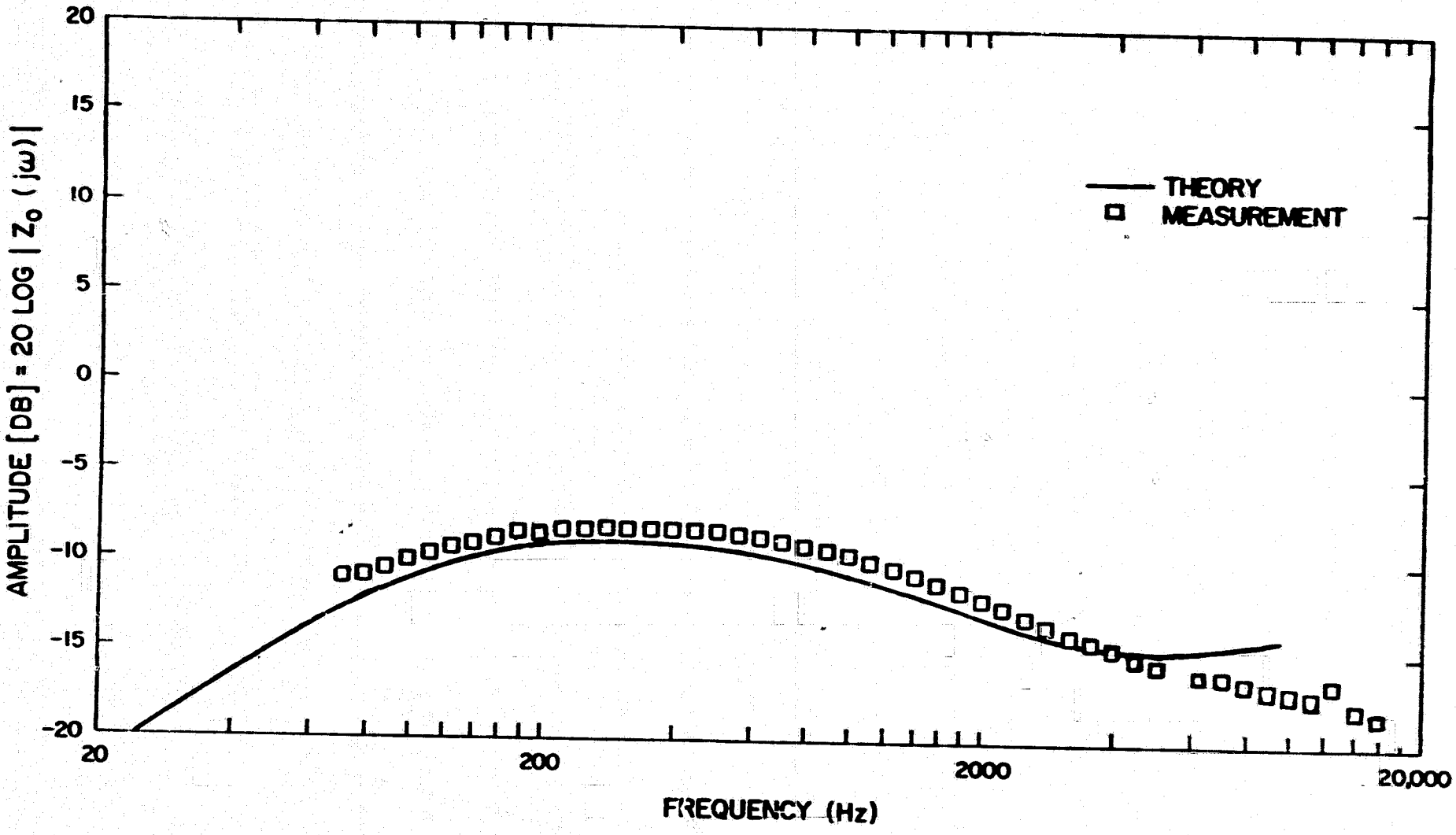


FIG. 6.4 OUTPUT IMPEDANCE CHARACTERISTIC OF THE BUCK CONVERTER IN *Example 1* DESIGN

STEP LOAD CHANGE

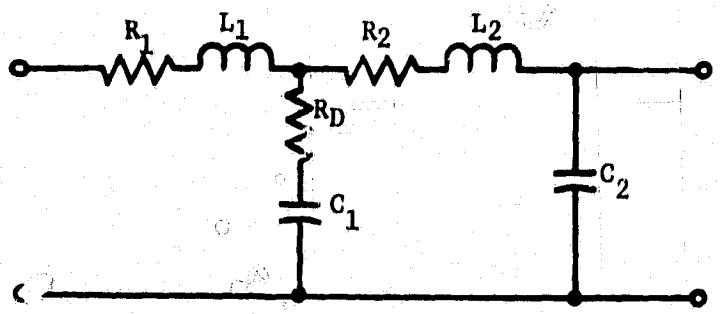
R_L = 10 OHMS ↔ 11 OHMS

VERTICAL SCALE: 0.1 V/DIV.
HORIZONTAL SCALE: 1 MSEC/DIV.

	THEORETICAL	MEASURED
SETTLING TIME	1.76 MS	1.8 MS
PEAKING	68 MV	60 MV

FIG. 6.5 STEP LOAD TRANSIENT RESPONSE IN *Example 1* DESIGN

Example 2. *Example 2* is the same as *example* 1 except that a two-stage input filter is employed as shown in the following figure.



R_1 = .2 ohm

L_1 = 325 μH

R_2 = .02 ohm

L_2 = 116 μH

C_1 = 200 μF

C_2 = 20 μF

R_D = 2ohm

The resonant frequency ω_1 is calculated:

$$\omega_1 = \frac{1}{\sqrt{L_1 C_1}} = 3922 \text{ rad/sec.}$$

The resonant peaking of $Z_F(j\omega)$ and $H_F(j\omega)$ are computed using equations from Ref. 11:

$$B_R = Z_F(j\omega_1) \cong \left\{\frac{L_1}{C_1}\left(1 + \frac{1}{R_D}\frac{L_1}{C_1}\right)\right\}^{1/2} = 1.71$$

$$B_F = H_F(j\omega_1) \cong \left\{\left(1 + \frac{R_D^2 C_1}{L_1}\right) / \left[\left(\frac{C_2}{C_1}\right)^2 + \frac{R_D^2 C_1}{L_1}\left(1 - \frac{C_2}{C_1} - \frac{L_2 C_2}{L_1 C_1}\right)^2\right]\right\}^{1/2}$$

$$= 1.51$$

It should be noted that only the resonant peaking at the first stage filter resonant frequency ω_1 is important. The peaking effect at the second stage resonant frequency, $\omega_2 = 1/\sqrt{L_2 C_2}$, is usually less severe than that of the first stage and is neglected for design purposes. The same design procedure used in the previous example is followed here except that *step 3*

is modified to include the effect of input filter resonant peaking.

$$s_{ol} \geq M_3 = \frac{\frac{K_2}{K_1}\omega_0}{K_A} \cdot \frac{B_F}{1 - B_R/(\mu^2 R_L)} = 1.17$$

This modification does not cause any change of the feasible range of α' derived in *step 7* of the previous example.

It should be noted that in this example the effect of the input filter interaction to the control loop is negligible since

$$Z_F(j\omega_1) = B_R = 1.71$$

and the negative resistance of the regulator

$$\mu^2 R_L = 62.5$$

Thus, $Z_F(j\omega_1) << \mu^2 R_L$.

The effect of the input filter to the audiosusceptibility can be computed easily in this example. The audiosusceptibility characteristic is increased at the input filter resonant frequency by an amount equal to

$$20 \log \frac{B_F}{1 - B_R/\mu^2 R_L} = 3.82 \text{ db.}$$

which checks very well with the experimental measurements as shown in Fig. 6.6.

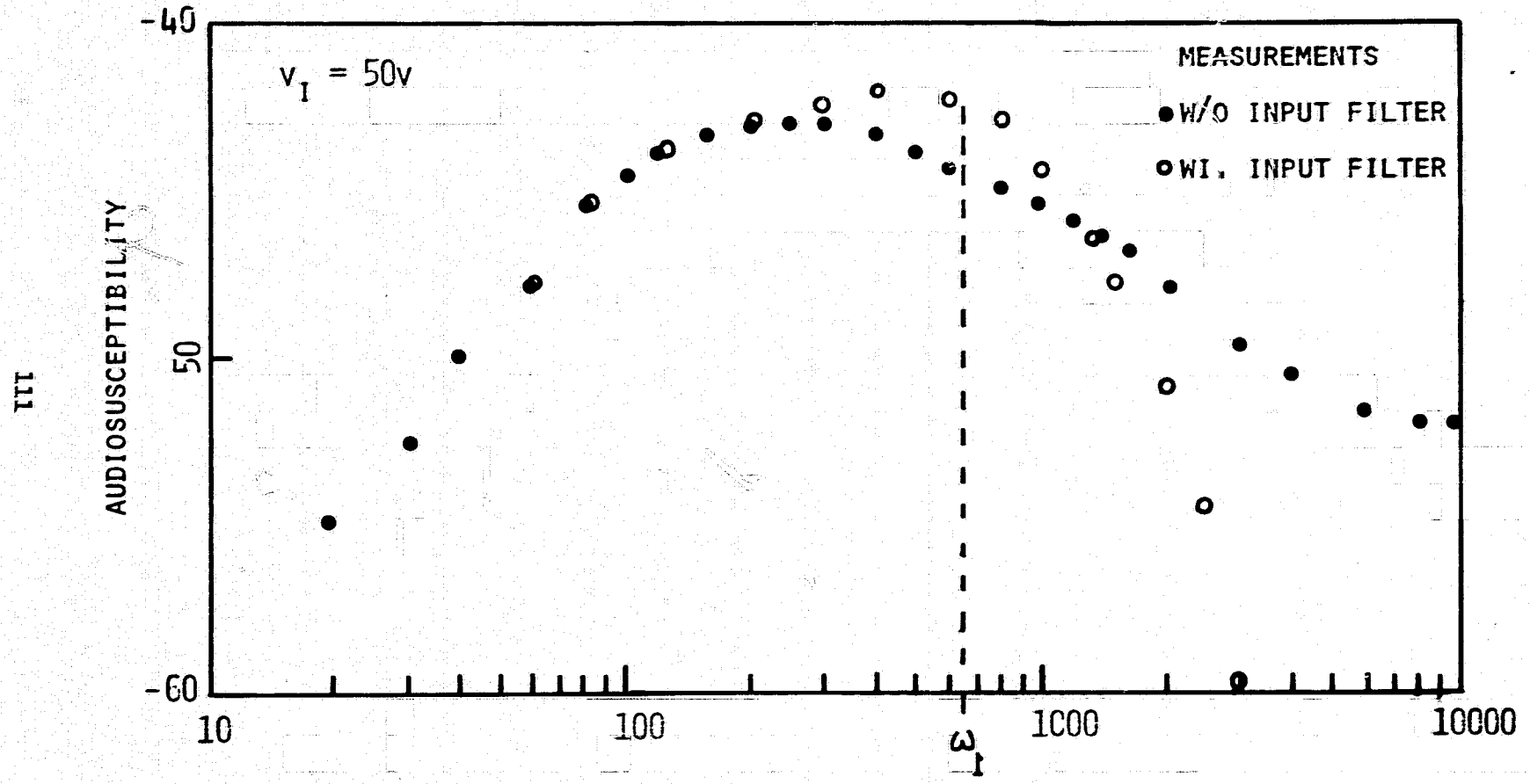


FIG. 6.6 MEASUREMENT OF THE AUDIOSUSCEPTIBILITY CHARACTERISTIC WITH AND WITHOUT AN INPUT FILTER IN *Example 2* DESIGN

Example 3: *Example 3* is the same as *example* 1 except for V_I and P_o which have the following ranges:

V_I = 30 to 50 volts

P_0 = 20 to 40 watts

The worst case usually occurs during a low-line and heavy-load condition. Under this condition,

V_I = 30 v

D = 0.667

D' = 0.333

$K_1 = 6.82 \times 10^4$

K_2 = 0.667

μ = 1.5

One can calculate:

M_1 = 1.751

M_2 = 2.094

M_4 = 1.751

Comparing the above parameter values with those derived in example 1, one can conclude that when the line voltage is reduced, the magnitude of M_2 increases while M_1 and M_4 remain unchanged. One concludes that when the line voltage is reduced, the audiosusceptibility degrades while the step load transient peaking and the output impedance remain unchanged.

The feasible ranges for s_{o1} and s_{o2} are determined from *Steps* 1 through 6.

$2.094 \leq s_{o1} \leq 13$

$0.131 \leq s_{o2}$

The previous design values

$$\alpha' = 0.355 \qquad \tau'_{z2} = 1.76 \times 10^{-3}$$

or

$$s_{o1} = 1.751 \qquad s_{o2} = 0.149$$

slightly violate the audiosusceptibility constraint.

If the input filter of example 2 is now added, all other parameters remaining the same, the lower bound for s_{o1} becomes $\text{Max}\{M_1, M_3, M_4\} = M_3 = 3.25$. Thus, the design values given above, with $s_{o1} = 1.751$, are no longer suitable. New values must be calculated to satisfy the design constraints.

Figure 6.7 shows the audiosusceptibility with an input filter when the control parameters $\alpha' = 0.335$ and $\tau'_{z2} = 1.76 \times 10^{-3}$ derived in *example 1* are employed. It is shown that the worst audiosusceptibility (-34.2 db) is greater than that specified in the design requirement.

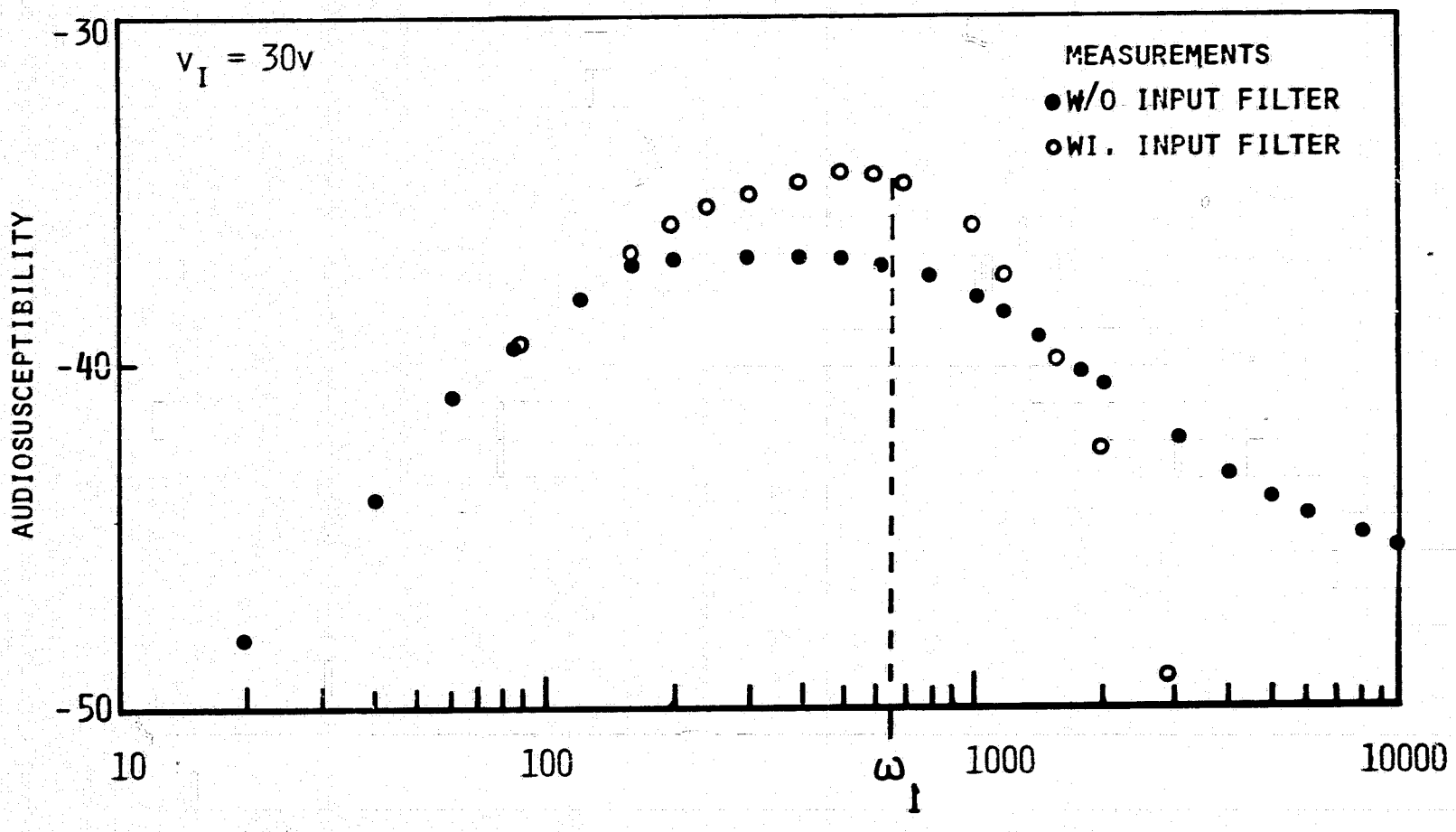


FIG. 6.7 MEASUREMENT RESULT OF THE AUDIOSUSCEPTIBILITY CHARACTERISTIC IN *Example 3* DESIGN

Example 4: Design the SCM control circuits for a buck/boost converter without an input filter.

Input-output requirements:

$V_I = 20$ volts

$V_o = 28$ volts

$D = .5833$

$D' = 0.4166$

$P_o = 28$ watts

Power stage parameters:

$L_s = 220\ \mu H$

$L_e = \frac{L_s}{D'^2} = 1267.6\ \mu H$

$C = 700\ \mu F$

$R_c = 0.05$ ohm

$R_e = 0.5$ ohm

$R_L = 28$ ohms

$\omega_o = 1.0616 \times 10^3$

$\zeta = 0.228$

$N_s = N_p$

Pulse modulator parameters:

$T_{ON} = 25\ \mu$ sec.

$M = V_I\ T_{ON} = 0.5 \times 10^{-3}$ volt-second.

Other key power stage parameters can be calculated:

$$\mu = \frac{N_p}{N_s} \frac{D'}{D} = 0.714$$

$$K_1 = \frac{2V_I}{M} = 8.\times 10^4$$

$$K_2 = \frac{1}{\mu} (1 + K_1 \frac{L_e}{R_L} D) = 4.358$$

$$A_2 = \frac{D}{cR_L} = 29.76 \quad , \qquad A_1 \approx 1$$

The design specifications are given as follows:

(1) The audiosusceptibility should be less than -35 db. for all frequencies, i.e. $K_A = 0.01778$.

(2) The output impedance should be less than 0.4 ohm for all frequencies, i.e. $K_o = 0.4$

(3) The phase margin at the crossover frequency should be greater than 70°.

(4) Load transient response:

(a) Time constant $\tau_s < 7.5 \times 10^{-3}$ sec.

(b) Output voltage peaking should be less than 0.2% of its nominal dc value for a 10% step change of the output current from its nominal value, i.e. $K_{op} = 0.02$.

(5) Dc regulation $K_{DC} \leq 5 \times 10^{-6}$.

Design procedures:

Step 1: Time constant of transient response is determined:

$$\tau'_{z2} \leq 7.5 \times 10^{-3} \text{ sec. or } s_{o2} \geq 0.125$$

Step 2: Step load transient peaking constraint:

$$s_{o1} \geq M_1 = 2.57$$

Step 3: Audiosusceptibility constraint:

$$s_{o1} \geq M_2 = 3.58$$

Step 4: Output impedance constraint:

$$s_{o1} \geq M_4 = 3.71$$

Step 5: The upper bound of s_{o1} is determined:

$$s_{o1} \leq \frac{1}{\omega_o \tau_{z1}} = 19.2$$

Step 6: Feasible range for s_{o1} and s_{o2} :

$$\max \{M_1, M_2, M_4\} \leq s_{o1} \leq 19.2$$

$$3.71 \leq s_{o1} \leq 19.2$$

$$s_{o2} \geq 0.125$$

Feasible range for the product $\alpha' \tau'_{z2}$:

$$3.49 \times 10^{-3} \leq \alpha' \tau'_{z2} \leq 1.81 \times 10^{-2}$$

Step 7: Choose $\tau'_{z2} = 7.5 \times 10^{-3}$ sec.

then $0.464 \leq \alpha' \leq 2.413$

Curves of gain and phase corresponding to this feasible range of α' are shown darkened in Fig. 6.8, the set of open-loop characteristics corresponding to $\omega_o \tau'_{z2} = 8$. (These curves are given again in Fig. A.9). The phase margin requirement may now be considered. As before, the vertical scale of Fig. 6.8(a) has been normalized by the factor $(K_1\alpha)/(\omega_o\alpha')$ so that a magnitude of $20 \log \left(\frac{K_1\alpha}{\omega_o\alpha'} \right)$ must be added to Fig. 6.8(a) to obtain the actual open-loop gain.

$$20 \log \frac{K_1\alpha}{\omega_o\alpha'} = 20 \log \frac{K_1}{\omega_o} + 20 \log \frac{\alpha}{\alpha'}$$

$$= 37.5 + 20 \log \frac{1}{1 + 0.106\alpha'}$$

For $\alpha' = 0.464$, $20 \log \frac{K_1\alpha}{\omega_o\alpha'} = 37.08$ db.

From Fig. 6.8 one can find that:

The crossover frequency $f_{x1} = 70\ f_o$

The phase margin $\theta_{x1} = 85°$

For $\alpha' = 2.413$, $20 \log \frac{K_1\alpha}{\omega_o\alpha'} = 35.5$ db.

The crossover frequency $f_{x2} = 65\ f_o$

The phase margin $\theta_{x2} = 75°$

The entire feasible range for α', derived in *Step 7* with $\tau'_{z2} = 7.5 \times 10^{-3}$ sec., satisfies the stability margin defined [illegible] design specification. It may appear to be desirable to [illegible] the

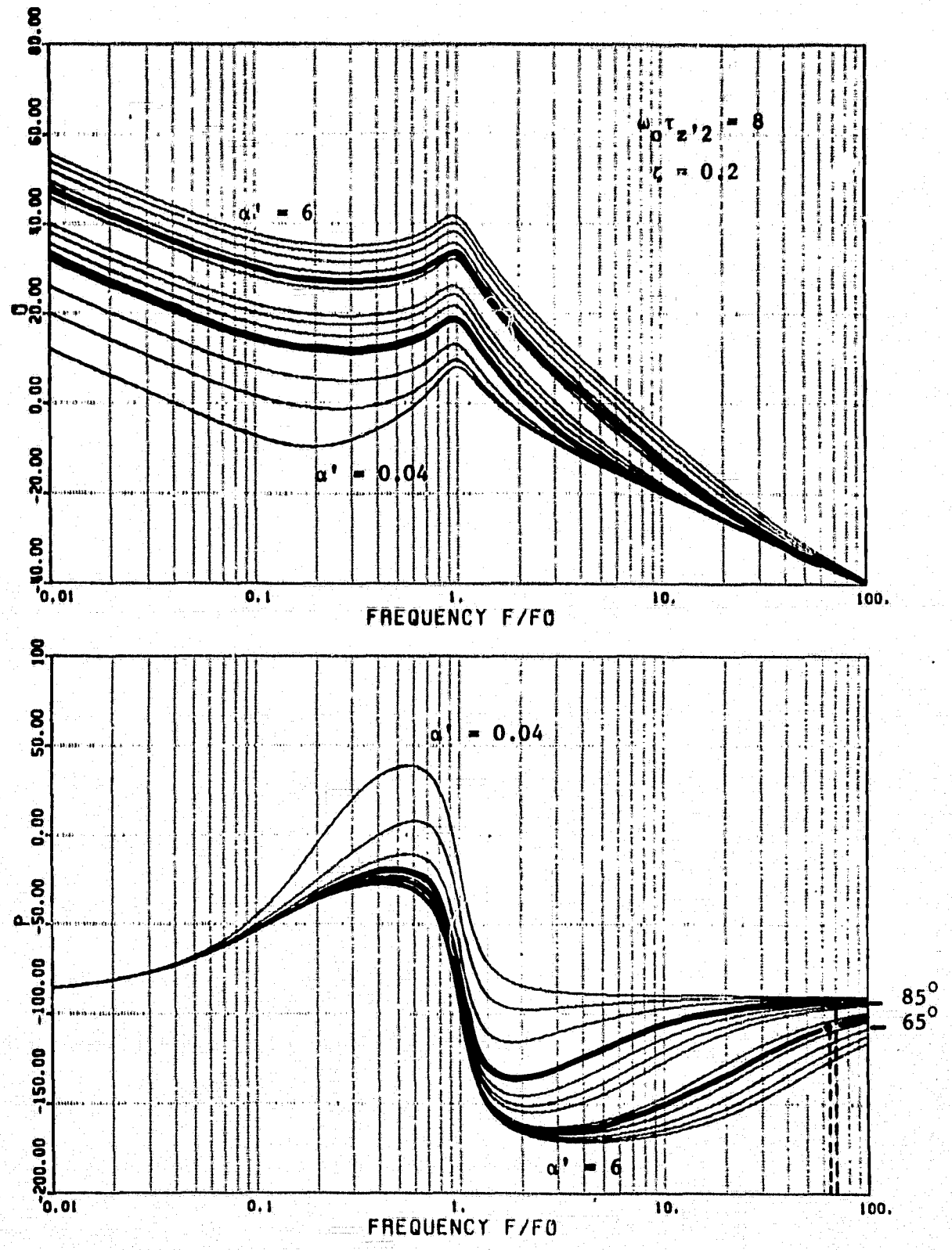


FIG. 6.8 DETERMINATION OF THE FEASIBLE RANGE FOR THE CONTROL PARAMETER α'.

largest possible α' (in this case $\alpha' = 2.41$) for optimum switching regulator performance. Since the upper bound of α' is determined by the temperature sensitive output filter capacitor ESR, however, a less than marginal selection of α' becomes desirable. Assuming that the output filter capacitor ESR could increase to 3 or 4 times its room temperature value while at low temperature, α' is chosen as

$$\alpha' = 0.71$$

From (3.15), $\alpha = 0.615$.

Step 8: Determine control circuit parameters:

$$R_1,\ R_2,\ R_3,\ R_4,\ R_5,\ C_1,\ C_2,\ n.$$

Since the number of unknowns are greater than the number of equations, the following parameter values are selected arbitrarily.

Let $E_R = 7$ volts

$R_1 = 43.2\ K\Omega$

$R_2 = 15\ K\Omega$

$$n = \frac{N_{AC}}{N_S} = \frac{22}{33} = 0.667$$

Employing $\alpha = 0.615$,

$$\frac{R_4}{R_3+R_x} = 0.68 \qquad \text{(A)}$$

Using the previously chosen value of τ'_{z2} ($=7.5 \times 10^{-3}$ sec.) gives

$$(R_5 + \frac{R_3+R_x}{g})C_2 = 7.5 \times 10^{-3} \qquad (B)$$

From (5.1), $R_5C_2 = R_cC = 3.5 \times 10^{-5}$ (C)

From (5.15) for $V_{T2} = 4^V$, $V_{T1} = 2^V$

$$R_4C_1 > 16.6 \times 10^{-5} \qquad (D)$$

From (5.14)

$$R_4C_1 \frac{R_4}{R_4+R_x+R_3} \geq \frac{n}{2} \frac{M}{Kg} \frac{F_I(o)}{F_D(o)} \frac{1}{K_{DC}}$$

or $$R_4C_1 \frac{R_4}{R_4+R_x+R_3} \geq \frac{12.7 \times 10^{-11}}{K_{DC}} \qquad (E)$$

The above five equations (A - E) can be used to solve for the five unknown R_4, R_3, R_5, C_1, and C_2 :

$R_4 = 40\ K\Omega$

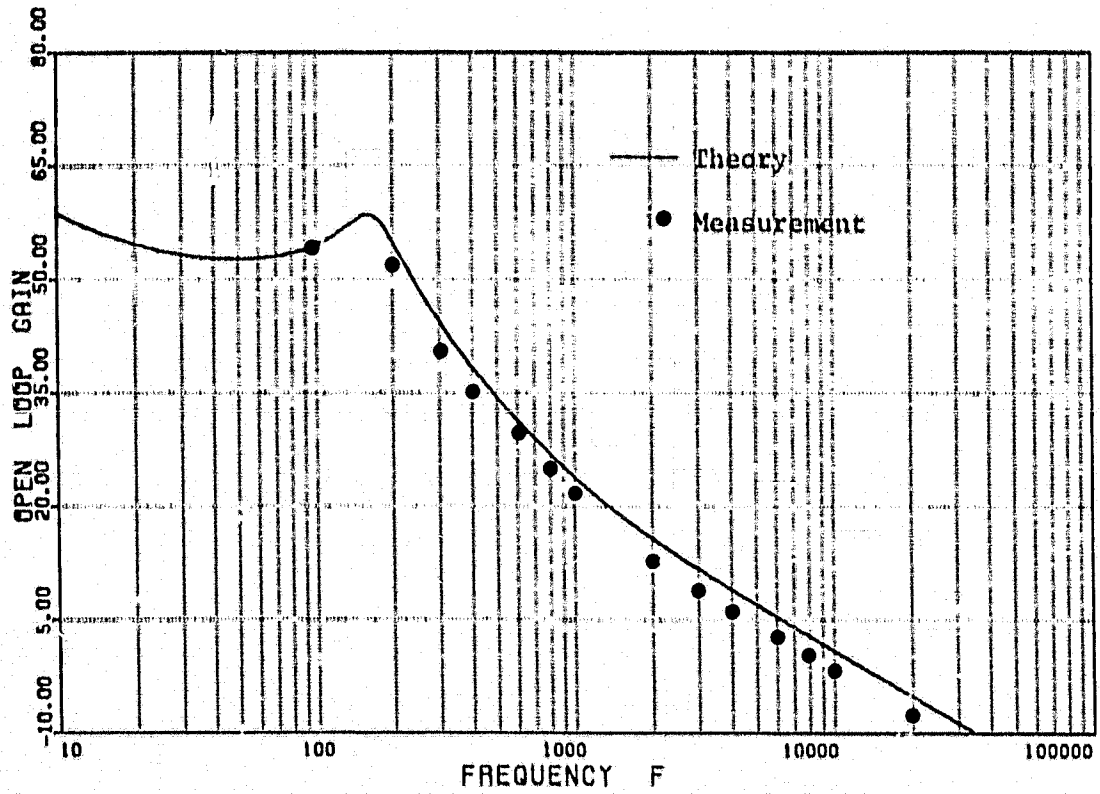
$R_3 = 47.5\ K\Omega$

$R_5 = 1.1\ K\Omega$

$C_1 = 5600\ PF$

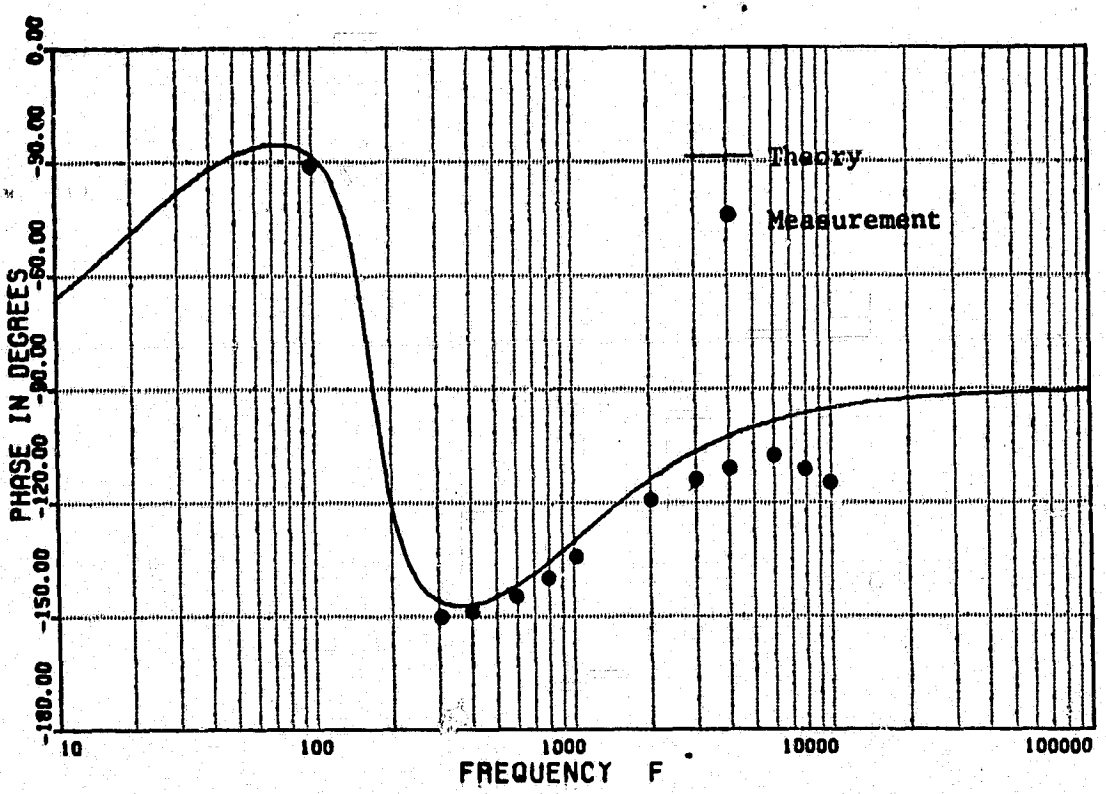
$C_2 = 32000\ PF$

To verify the design using this set of parameters, $\alpha = 0.65$, and $\tau'_{z2} = 7.5 \times 10^{-3}$ sec., one can examine the open loop, audiosusceptibility, output impedance, and step-load transient characteristics, which are shown in Fig. 6.9, 6.10, 6.11, and 6.12, respectively. Examining the test result summarized in Table 6.2, it is obvious that the design satisfies all the requirements.



(a)

FIG. 6.9(A) OPEN LOOP GAIN, THEORY AND MEASUREMENT, OF THE BUCK/BOOST CONVERTER IN *Example 4* DESIGN



(b)

FIG 6.9(B) OPEN LOOP PHASE, THEORY AND MEASUREMENT, OF THE BUCK/BOOST CONVERTER IN *Example 4* DESIGN

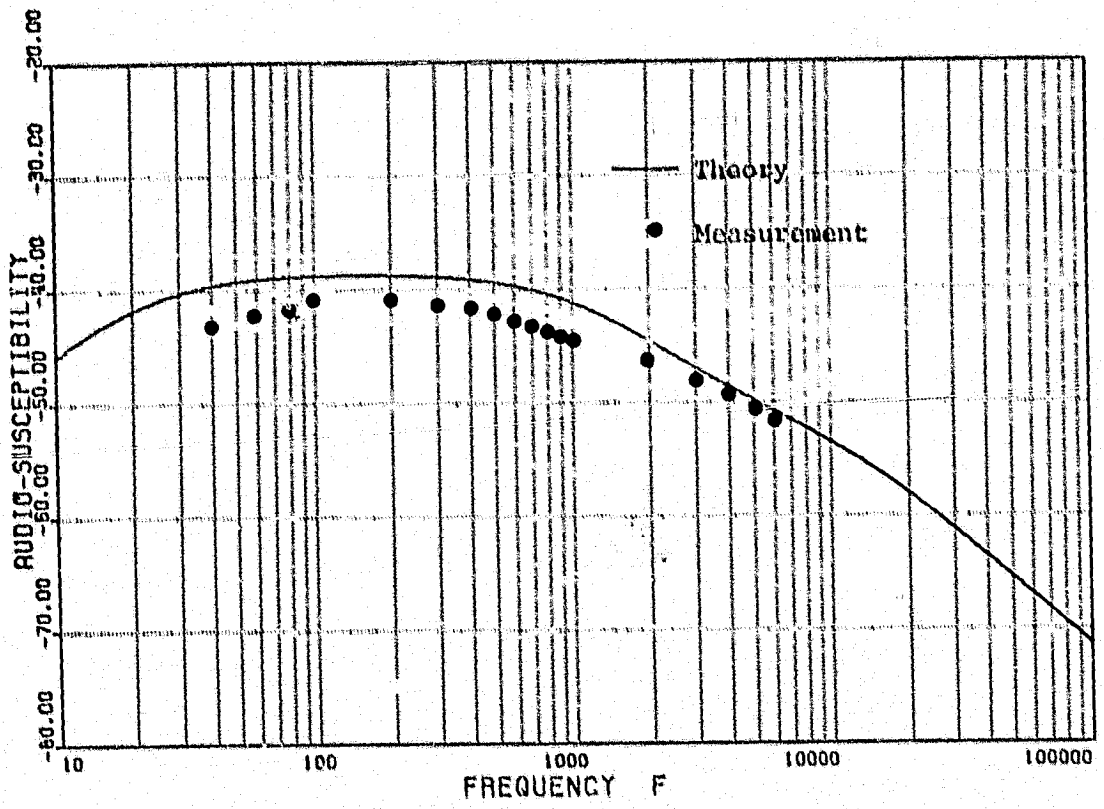


FIG. 6.10 AUDIO-SUSCEPTIBILITY CHARACTERISTIC THEORY AND MEASUREMENT, IN *Example 4* DESIGN

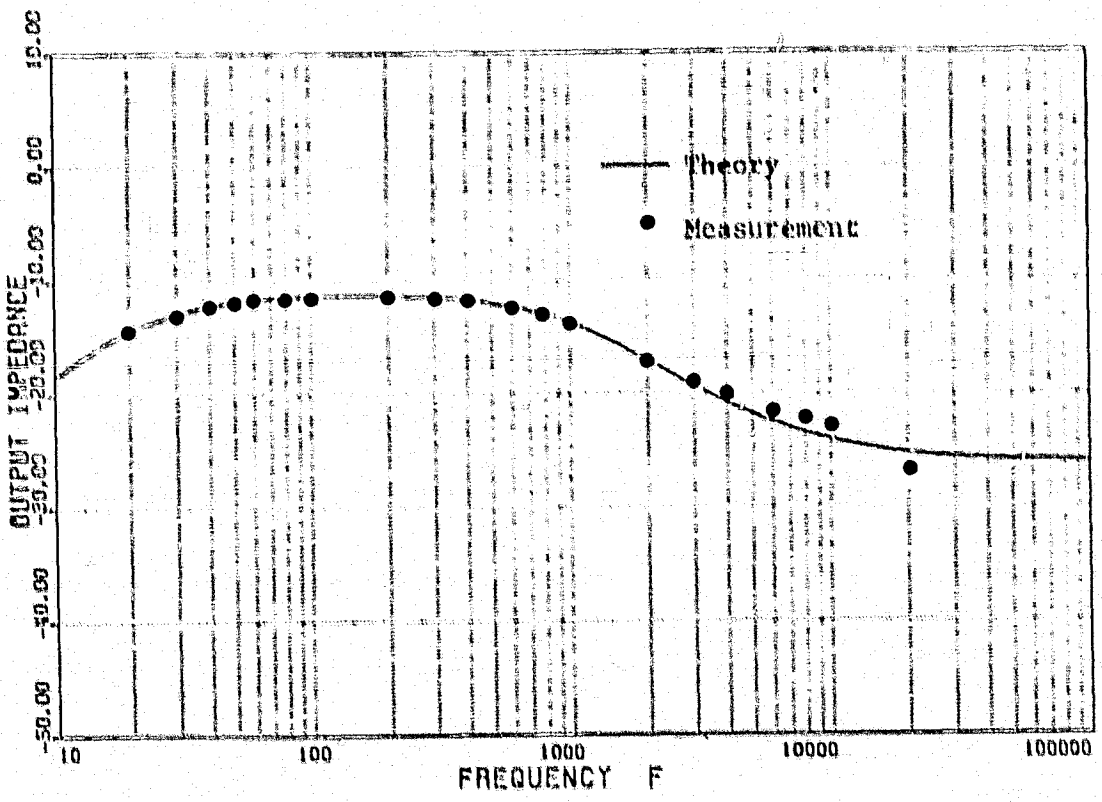
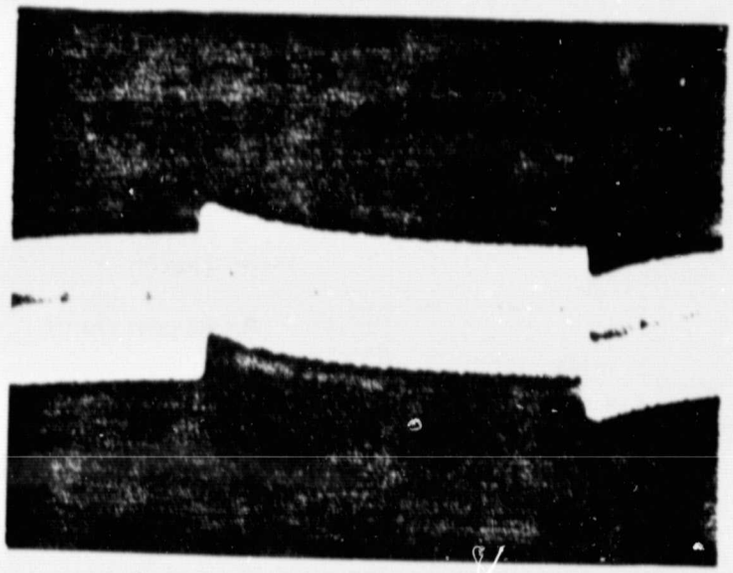


FIG. 6.11 OUTPUT IMPEDANCE CHARACTERISTIC, THEORY AND MEASUREMENT, IN *Example 4* DESIGN

STEP LOAD CHANGE

R_L = 28 OHMS ↔ 23 OHMS



VERTICAL: 0.1 V/DIV.

HORIZONTAL: 1 MS/DIV.

FIG. 6.12 STEP LOAD TRANSIENT RESPONSE IN *Example 4* DESIGN

TABLE 6.2 SUMMARY OF THE BUCK/BOOST CONVERTER PERFORMANCES
(THEORY AND MEASUREMENT)

	THEORY	MEASUREMENT	SPECIFICATION
CROSSOVER FREQUENCY (HZ)	10000	8000	N/A
PHASE MARGIN	85^0	70^0	70^0
AUDIO-SUSCEPTIBILITY (DB)	-38.5	-40	-35
OUTPUT IMPEDANCE (OHM)	0.26	0.26	0.4
TRANSIENT SETTLING TIME (MS)	7.5	7.5	7.5*
TRANSIENT PEAKING $(\Delta V_0/V_0)/(\Delta I_0/I_0)$	0.0095	0.009	0.02

CHAPTER VII

CONCLUSIONS

Three basic switching regulators, buck, boost, and buck/boost, each employing a Standardized Control Module (SCM), were characterized by a common small-signal block diagram in Volume I of this report, "Application Handbook for a Standardized Control Module for DC-DC Converters." Employing this unified model, regulator performances such as stability, audiosusceptibility, output impedance, and step-load transient response were analyzed, and key performance indices were expressed in simple analytical forms. A simple, unified procedure was then realized in Volume II, the User's Handbook. This procedure enables the user to select the key SCM Control parameters for arbitrarily given power-stage configurations and parameter values such that all regulator performance specifications can be met and optimized concurrently in a single design attempt.

Presented in Chapter II of the User's Design Handbook are the circuit descriptions of the SCM including the standardized Analog Signal Processor and Digital Signal Processor. The merits of SCM control are briefly summarized according to the following categories:

(1) Ability to perform different duty-cycle control modes.

(2) Ability to provide power-component stress limitations.

(3) Ability to provide stabilization against output-filter parameter changes.

(4) Ability to provide adaptive compensation to the moving poles.

(5) Ability to shift the zero from the right-half s-plant to the left-half s-plane.

(6) Ability to provide unified design approach.

In Chapter III, all key results and performance indices, derived in Volume I and relevant to the SCM design, are concisely presented to facilitate frequent user reference. Included in this chapter are the high-lights of the stability analysis, audiosusceptibility analysis, output impedance analysis, step-load transient analysis, and DC regulation analysis. In each analysis, key performance indices are summarized, and theoretical limitations of each performance category are identified and expressed in simple analytical form. Based on the analytic results, practical design ranges for SCM control circuit parameters are readily identified, facilitating easy selection of proper control parameter values in order to optimize regulator performances.

In Chapter IV, the effects of the input filter are discussed, and input filter design considerations are presented. Following the suggested input filter design guidelines allows the detrimental effects of the input filter on regulator stability, output impedance, and load transient to be minimized and for all practical purposes neglected. The effect of an input filter on the regulator audiosusceptibility, however, cannot be neglected, and is expressed in a simple analytical form ready to be incorporated into the SCM design procedure.

In Chapter V, the key power stage parameters and SCM parameters are identified. Switching regulator performance specifications are presented in the form of design constraints and the basic design assumptions are stated. The design objective is defined as determining the set of SCM parameters, given the power stage parameters and duty cycle control means, such that the prescribed design constraints are satisfied and switching regulator performance is optimized.

Finally, easy to follow step-by-step design procedures are presented in Chapter VI. The simple unified design procedure is applied to four design examples covering buck and buck/boost converters including an input filter. Excellent correlations are shown among the design results, specified performance characteristics, and theoretical predications. Thus, for the first time, a single, non-iterative design procedure is presented to allow easy selection of the key control circuit parameters such that all specified regulator peformances may be met and optimzed concurrently.

CHAPTER VIII

REFERENCES

[1] F. C. Schwartz, "Analog Signal to Discrete Time Interval Converter (ASDTIC)" U.S. Patent 3,659, 184, 1972.

[2] A. D. Schoenfeld and Y. Yu, "ASDTIC Control and Standardized Interface Circuits Applied to Buck, Parallel, and Buck/Boost DC-DC Power Converters," NASA Report CR-121106, 1973.

[3] Y. Yu, R. I. Iwens, F. C. Lee, L. Y. Inouye, "Development of A Standardized Control Module For DC-DC Converters" NASA Contract Report, NAS3-18918, prepared by TRW Defense and Space System Groups, August 30, 1977.

[4] F. C. Lee and Y. Yu, "An Adaptive-Control Switching Buck Regulator-Implementation Analysis and Design," IEEE Trans. Aerospace and Electronic System, Vol. AES-16, No. 1, January 1980.

[5] F. C. Lee, Y. Yu and M. F. Mahmoud, "A Unified Analysis and Design Procedure for A standardized Control Module for DC-DC Switching Regulators," IEEE Power Electronics Specialists Conference, Record, 1980.

[6] M. F. Mahmoud and F. C. Lee, "Analysis and Design of an Adaptive Multi-Loop Controlled Two-Winding Buck/Boost Regulator," Proceedings of the International Telecommunication Energy Conference, September, 1979.

[7] M. F. Mahmoud, "Analysis and Design of an Adaptive Multi-Loop Controlled Two-Winding Buck/Boost Regulator," Masters Thesis, Virginia Polytechnic Institute and State University, Electrical Engineering Department, 1979.

[8] Y. Yu, F. C. Lee, J. Kolecki, "Modeling and Analysis Power Processing Systems," IEEE Power Electronics Specialists Conference, Record, 1980.

[9] G. W. Wester, "Low Frequency Characterization of Switched dc-dc Converters," Ph.D. Thesis Califronia Institute of Technology.

[10] R. D. Middlebrook and S. Cuk, "A General Unified Approach to Modeling Switching-Converter Power Stages," IEEE Power Electronics Specialists Conference, Record, 1976.

[11] F. C. Lee and Y. Yu, "Input Filter Design for Switching Regulators," IEEE Trans. on Aerospace and Electronic Systems, Vol. AES-15, No. 5, September 1979.

[12] R. D. Middlebrook, "Input Filter Consideration in Design and Application of Switchign Regulators," Proceedings of the IEEE Industry Application Society Annual Meeting, 1976.

[13] R. D. Middlebrook, "Design Techniques for Designing Input Filter Oscillation in Switching-Mode Regulators," Proceedings of the Fifth National Solid State Power Conversion Conference, 1978.

CHAPTER IX

APPENDIX

A.1 The Effect of The Output Filter Damping Constant ζ.

The effect of the damping constant ζ on the open loop characteristics is illustrated in Fig. A.1. The following parameter values are used: $\omega_o\tau'_{z2} = 5$, $\alpha' = 1$, and $\zeta = 0.05$, 0.1, 0.2, 0.3, 0.4, and 0.5. The effect of the damping constant on the open-loop gain and phase is shown only within one decade of the output filter resonant frequency. Since the open-loop crossover frequency is usually high (about 1/3 to 1/2 of the switching frequency), the stability margins are unaffected by the damping ratio for all practical purposes.

A.2 The Effect of The Control Parameters α' and τ'_{z2}.

The key control circuit parameters α' and τ'_{z2} are related to the zeros s_{o1} and s_{o2} of the open-loop transfer function according to eq. (5.2). These two parameters are responsible for all the control-dependent, small-signal regulator performances.

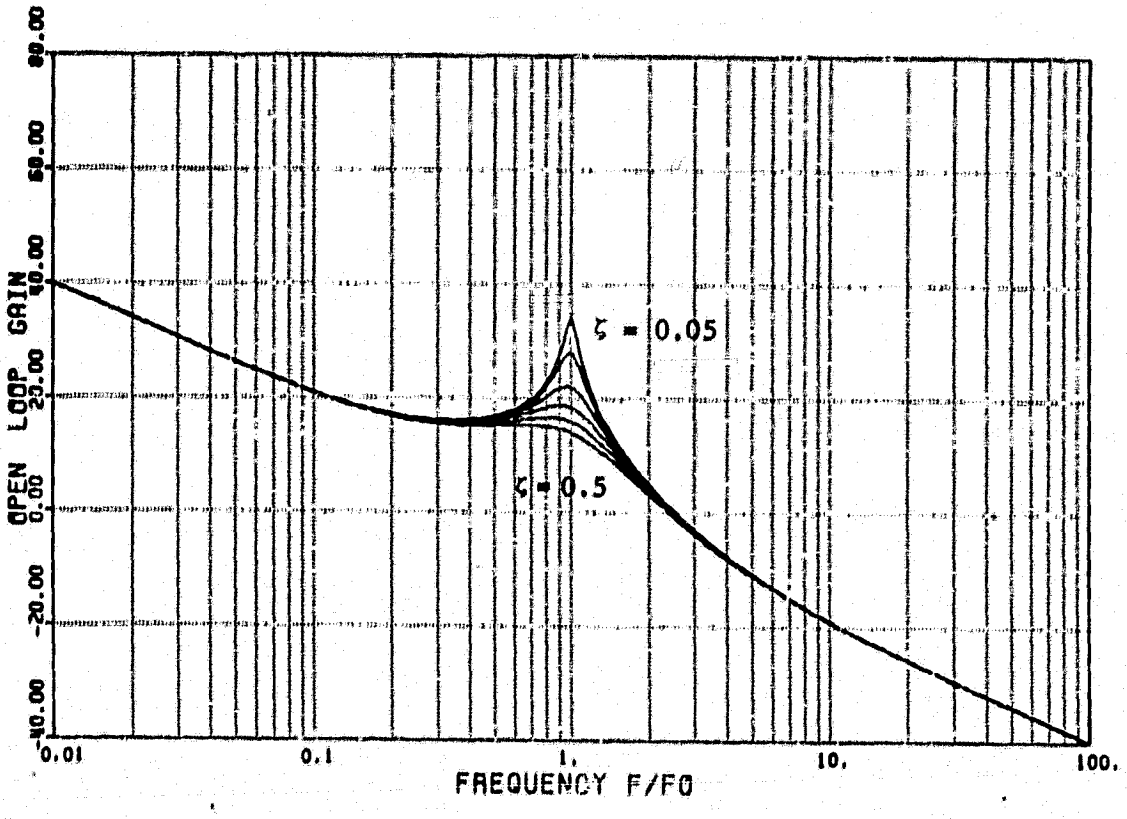
Curves are provided to facilitate the designer in selecting proper α' and τ'_{z2} for desirable crossover frequency and phase margin (*Step 7* of the design procedure; Section 6.1). Figures A.2 through A.11 show the set of open-loop gain and phase curves with specified $\omega_o\tau'_{z2}$ values ranging from 1 to 10. For each figure twelve α' values (0.04, 0.1, 0.2, 0.4, 0.6, 0.8, 1, 2, 3, 4, 5, and 6) are employed.

The normalized open-loop transfer function is employed for the various curves from Fig. A.2 to A.11. This normalized transfer function $G_T^*(s)$ is defined by the equation

$$G_T^*(s) \equiv \frac{G_T(s)}{\left(\frac{K_1\alpha}{\omega_o\alpha'}\right)} = \frac{\frac{1}{\alpha'}s^2 + \tau'_{z2}\omega_o s + 1}{s^2 + 2\zeta s + 1}\,\alpha' \qquad (A.1)$$

Values on the vertical scale of the gain plots are divided by the normalization factor $\frac{K_1\alpha}{\omega_o\alpha'}$ so that the families of curves shown in Figures A.1 through A.11 are applicable to all three types of switching regulators.

As described in *Step 7* of the design procedure, when the particular $\omega_o\tau'_{z2}$ value is chosen, based on the load transient requirement, the open-loop characteristic curve corresponding to the chosen $\omega_o\tau'_{z2}$ value is selected from Fig. A.2 to A.11. From this curve, the α' value can be determined in order to provide adequate crossover frequency and phase margin.



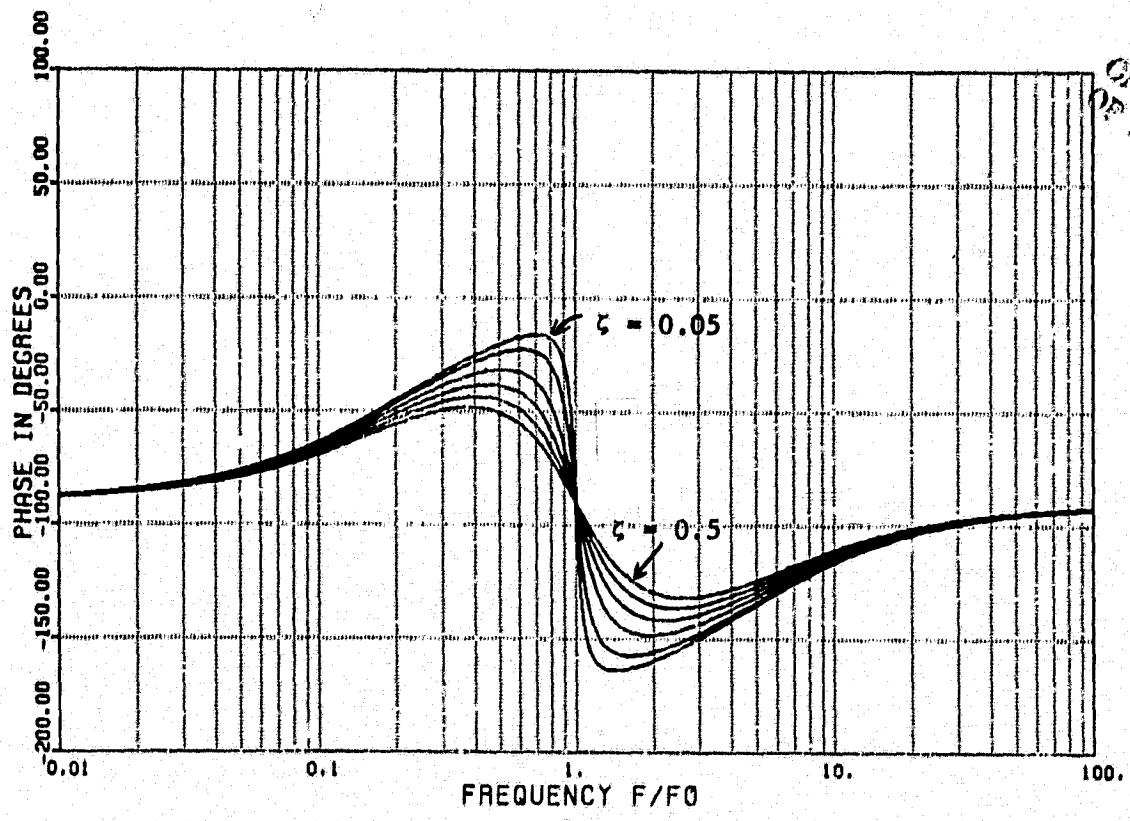


FIG. A.1 OPEN LOOP CHARACTERISTICS EMPLOYING $\alpha' = 1$, $\omega_o \tau'_2 = 5$ AND $\zeta = 0.05, 0.1, 0.2, 0.3, 0.4, 0.5$

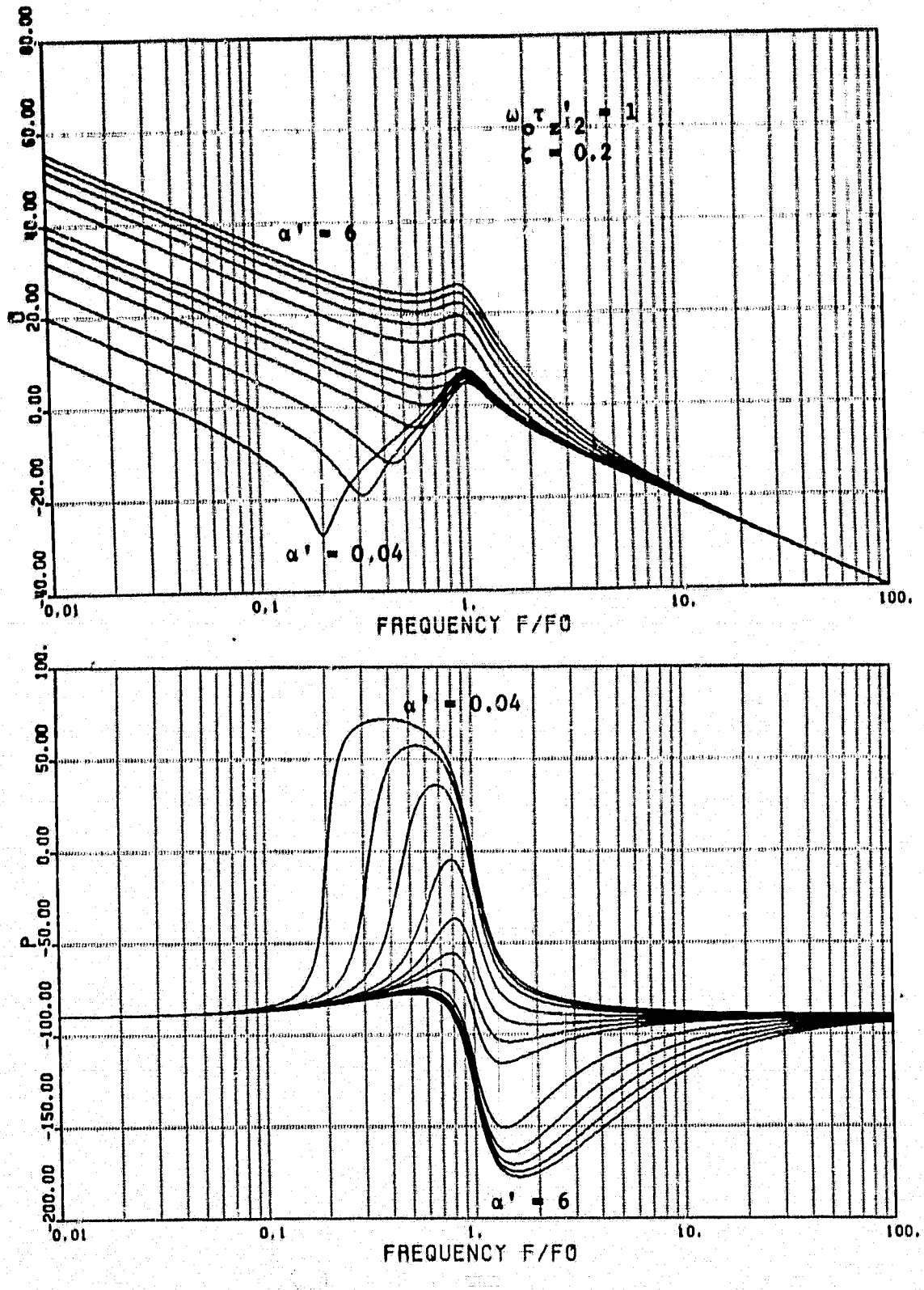
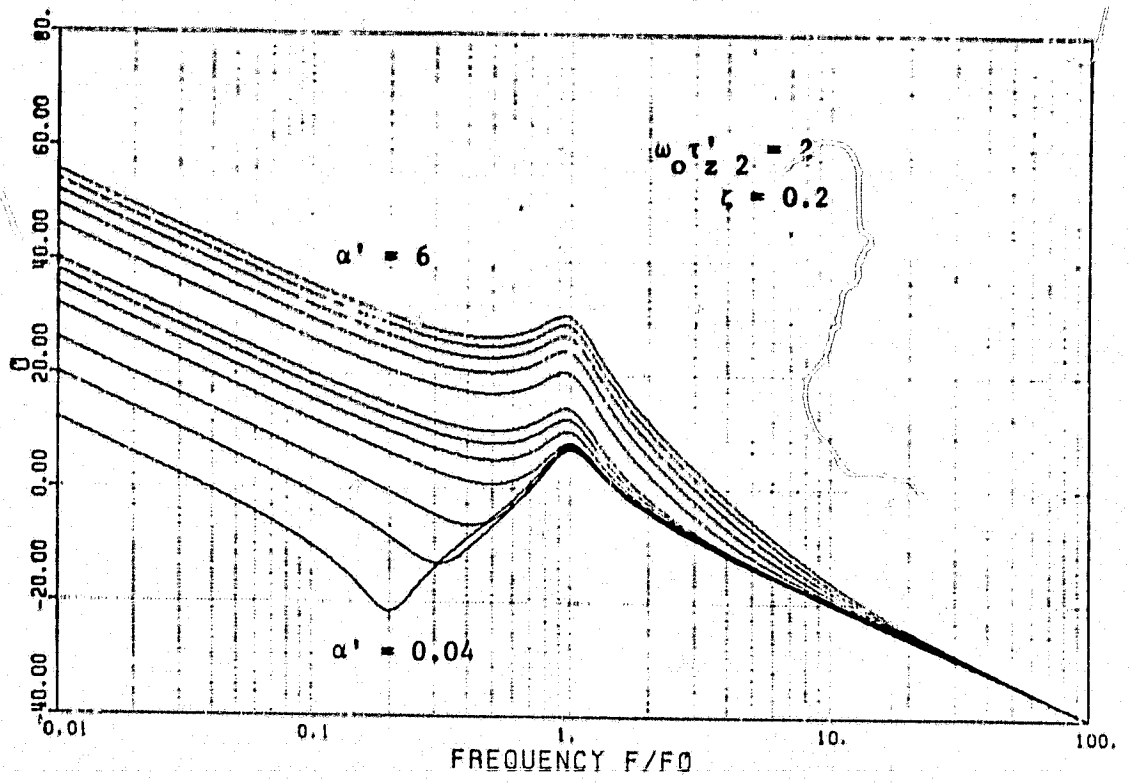


FIG. A.2 OPEN LOOP CHARACTERISTICS FOR $\omega_0\tau'_2 = 1$, $\zeta = 0.2$ AND $\alpha' = 0.04, 0.1, 0.2, 0.4, 0.6, 0.8, 1, 2, 3, 4, 5, 6$



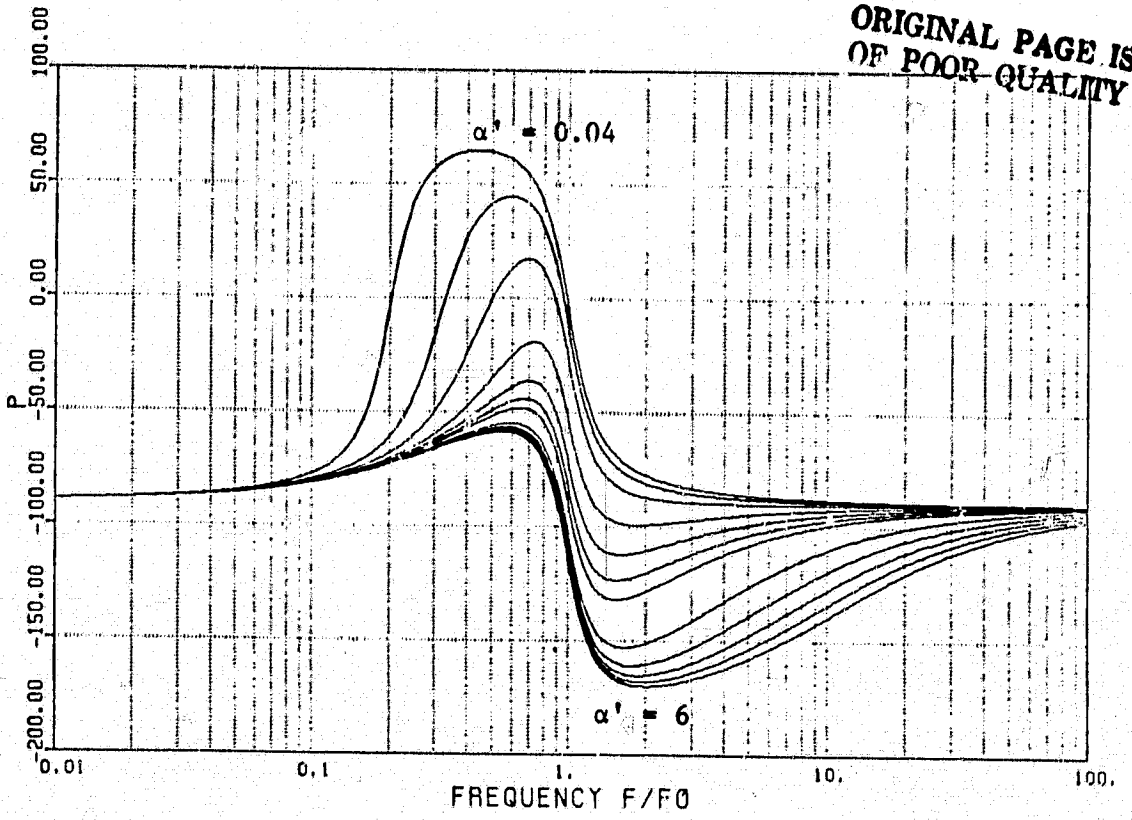


FIG. A.3 OPEN LOOP CHARACTERISTICS FOR $\omega_o\tau'_{z\,2} = 2$

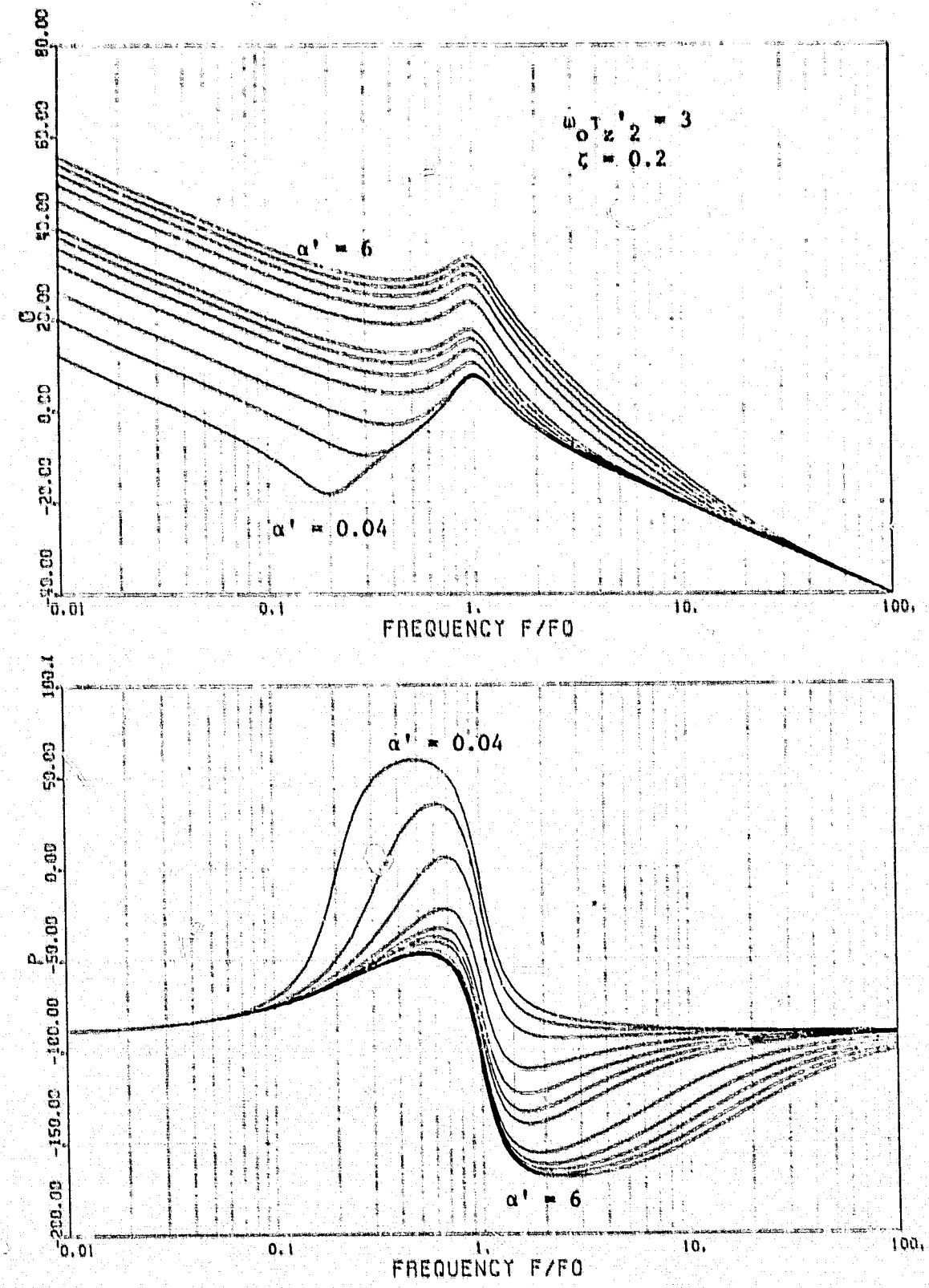
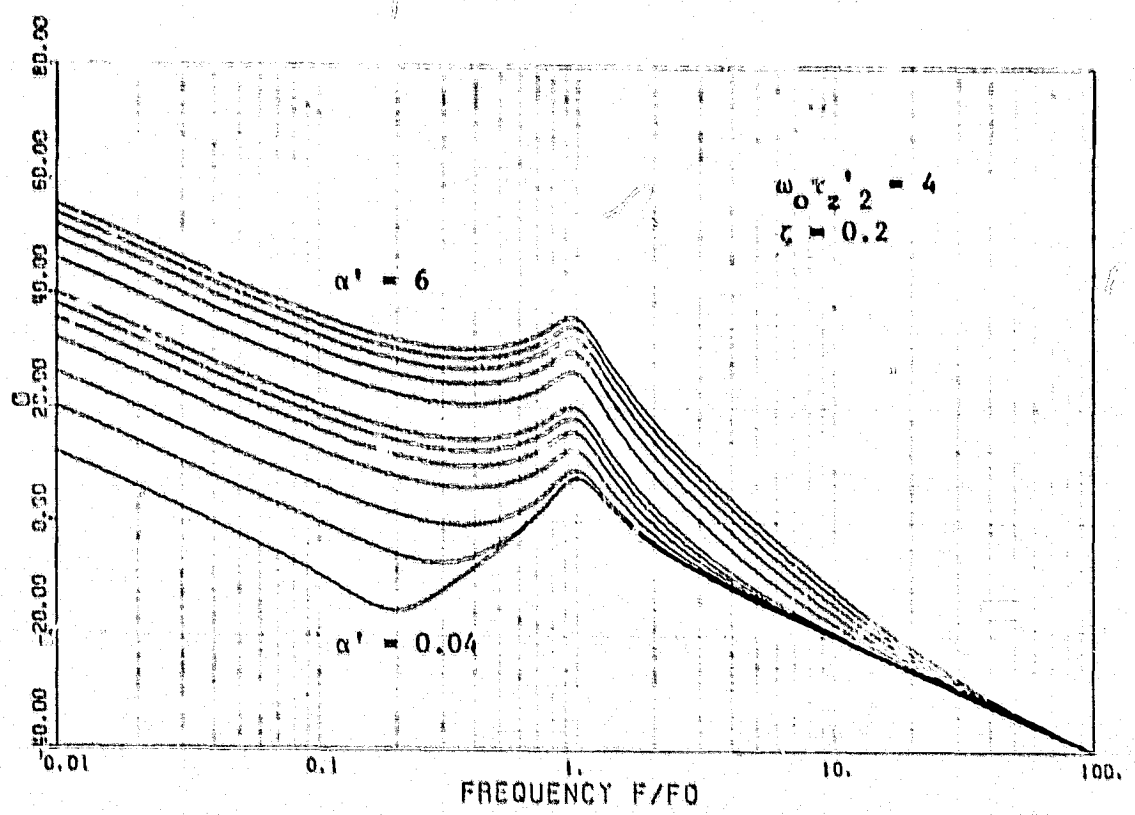


FIG. A.4 OPEN LOOP CHARACTERISTICS FOR $\omega_o \tau_{z'2} = 3$



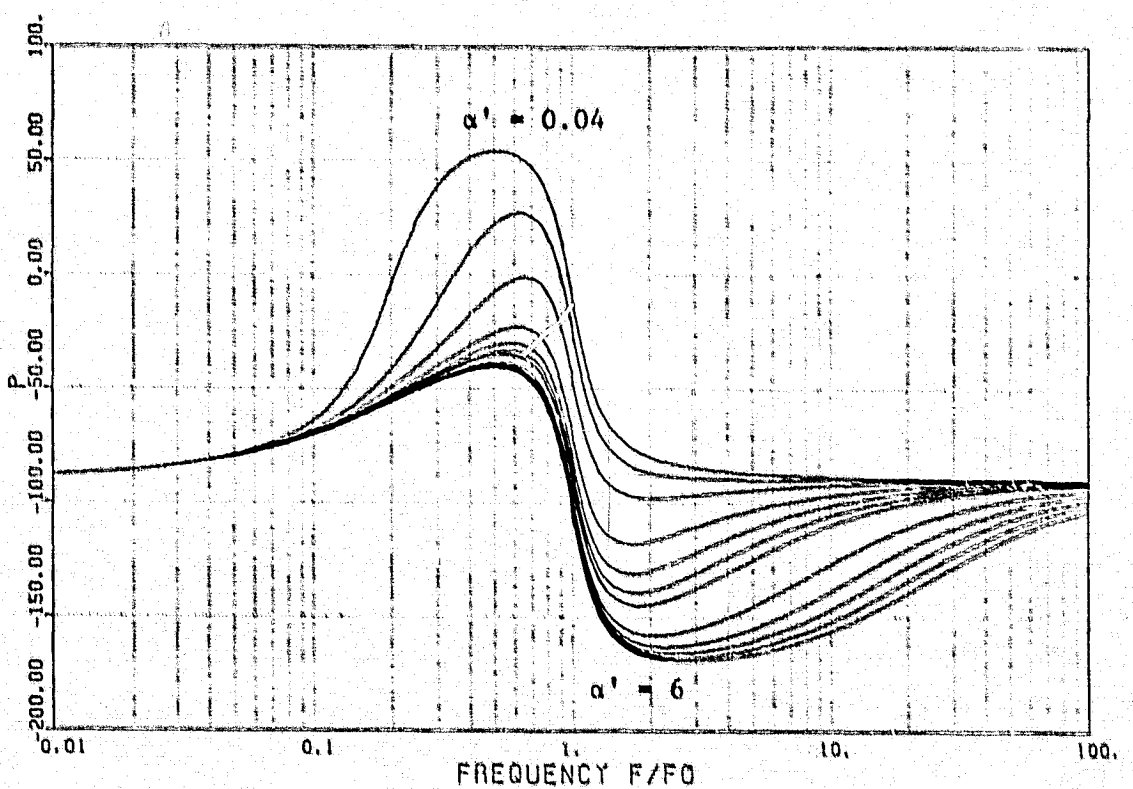


FIG. A.5 OPEN LOOP CHARACTERISTICS FOR $\omega_o \tau'_{z\,2} = 4$

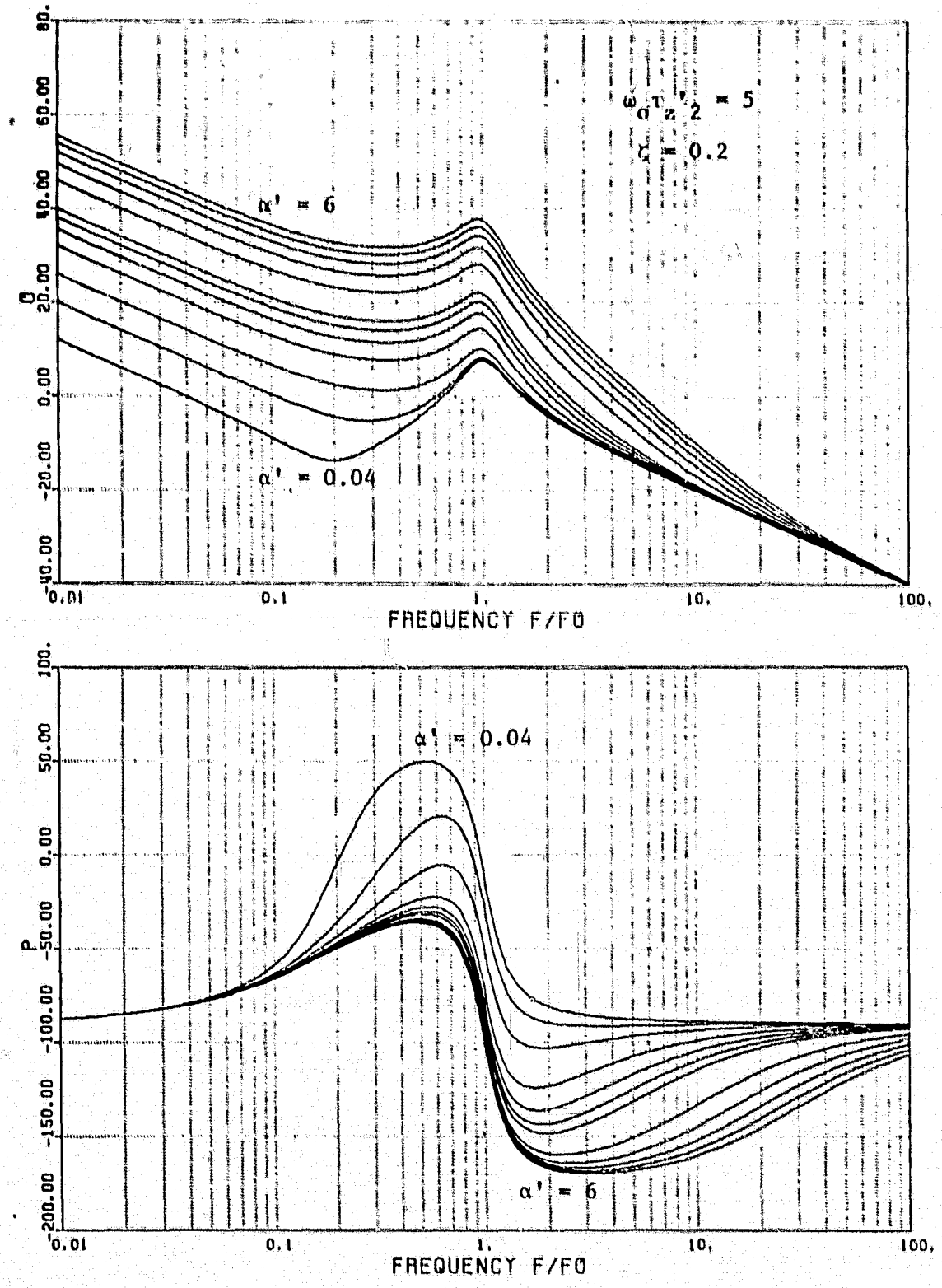
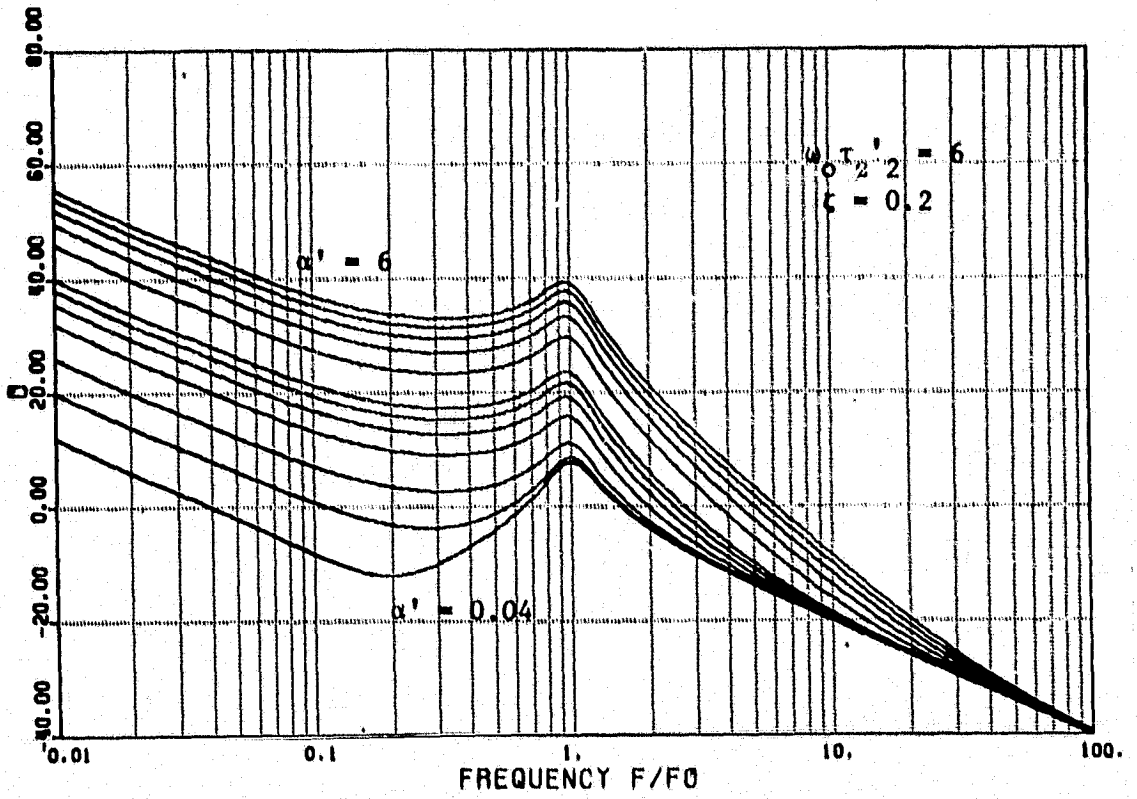


FIG. A.6 OPEN LOOP CHARACTERISTICS FOR $\omega_0 \tau'_{Z2} = 5$



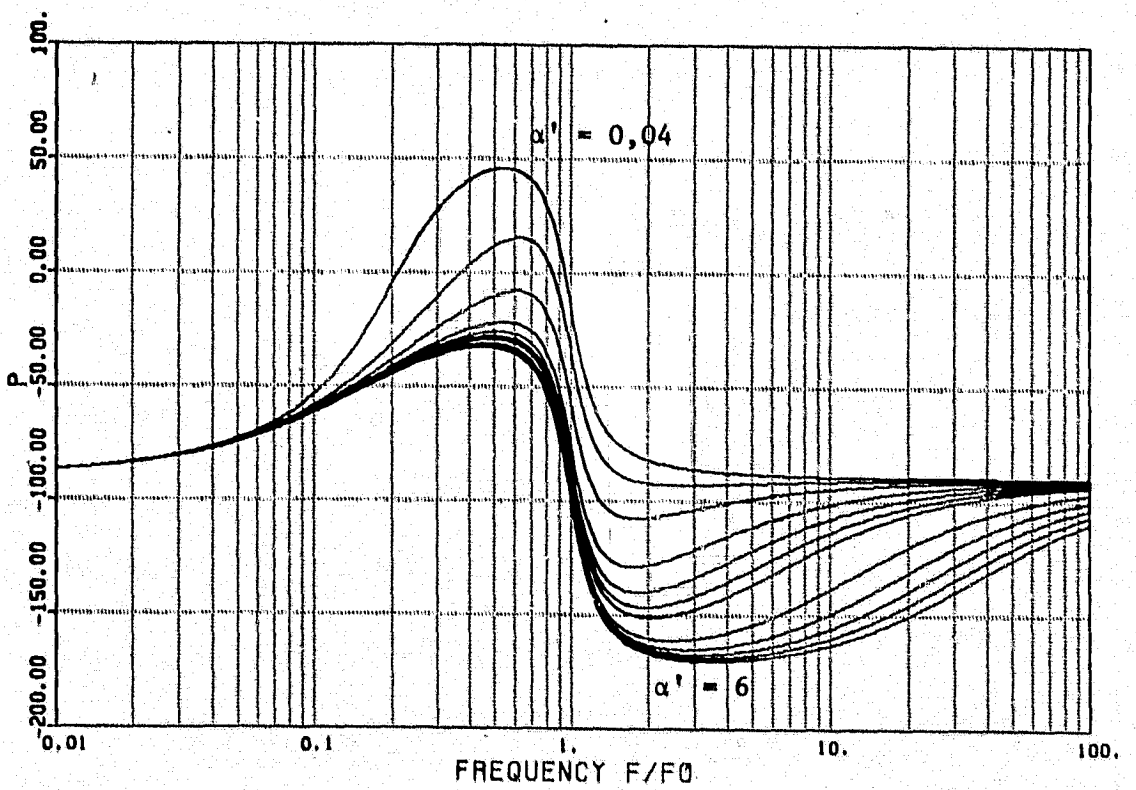


FIG. A.7 OPEN LOOP CHARACTERISTICS FOR $\omega_0 \tau_2' = 6$

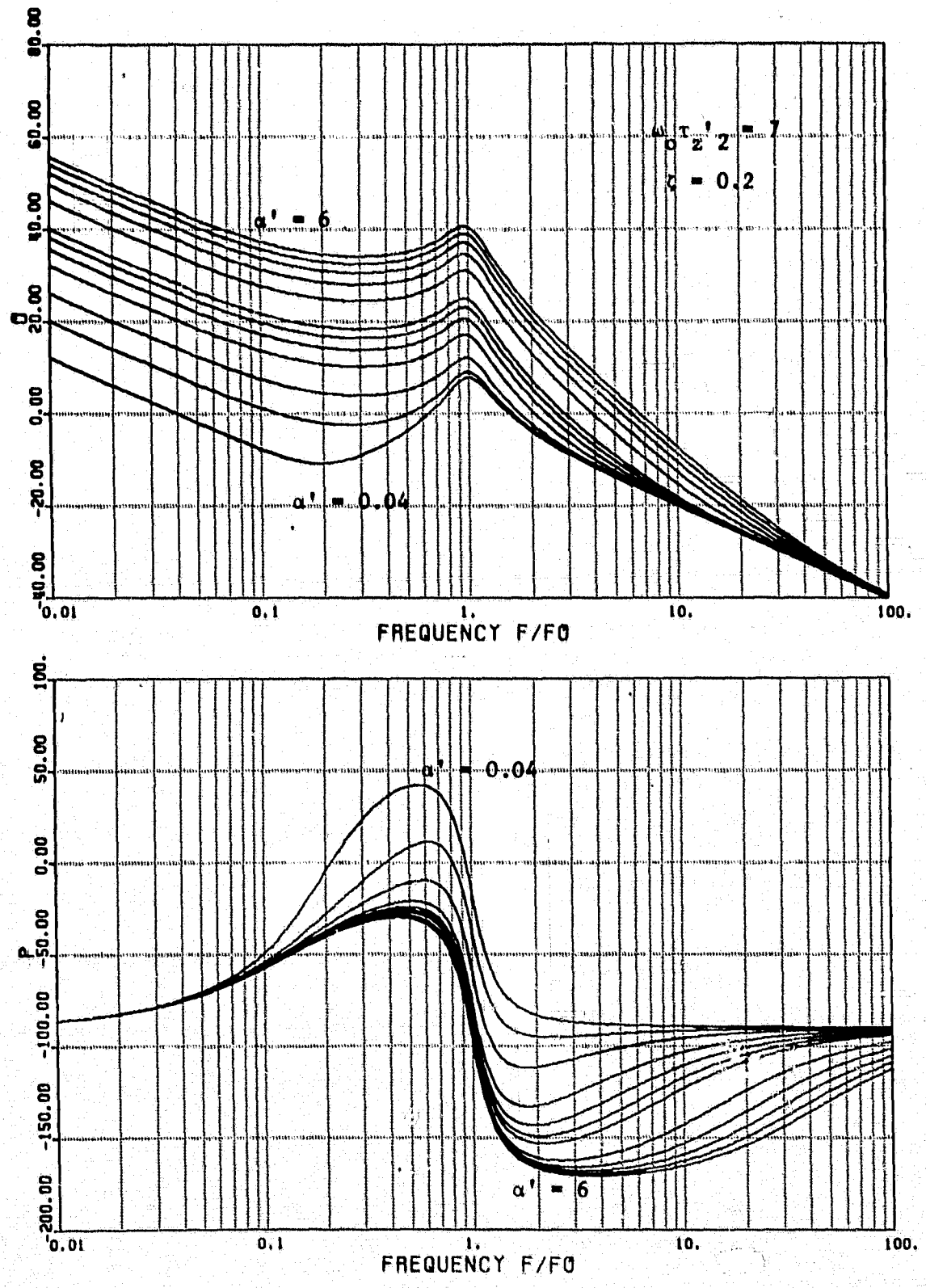


FIG. A.8 OPEN LOOP CHARACTERISTICS FOR $\omega_0 \tau'_{z\,2} = 7$

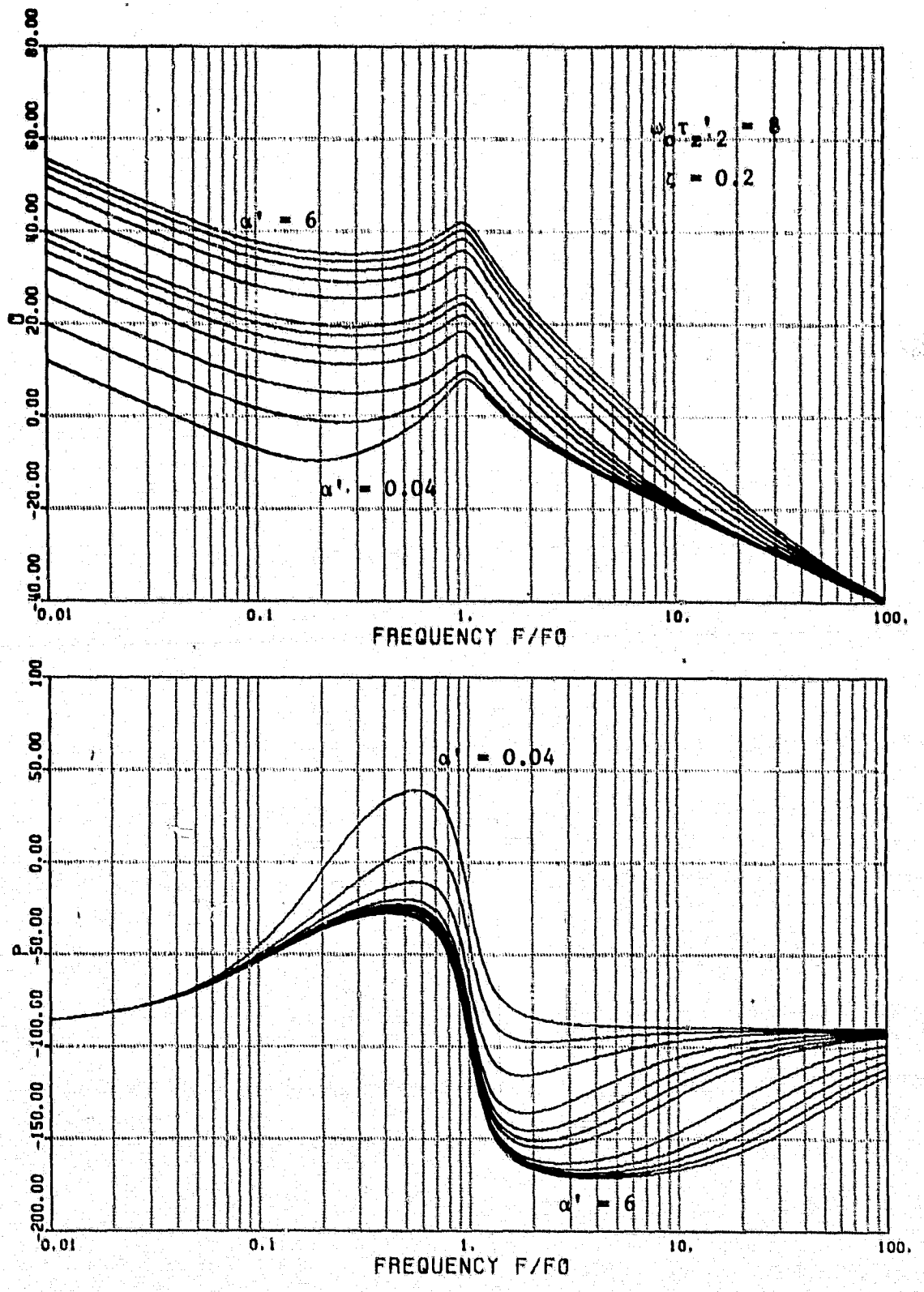


FIG. A.9 OPEN LOOP CHARACTERISTICS FOR $\omega_0 \tau'_{Z2} = 8$

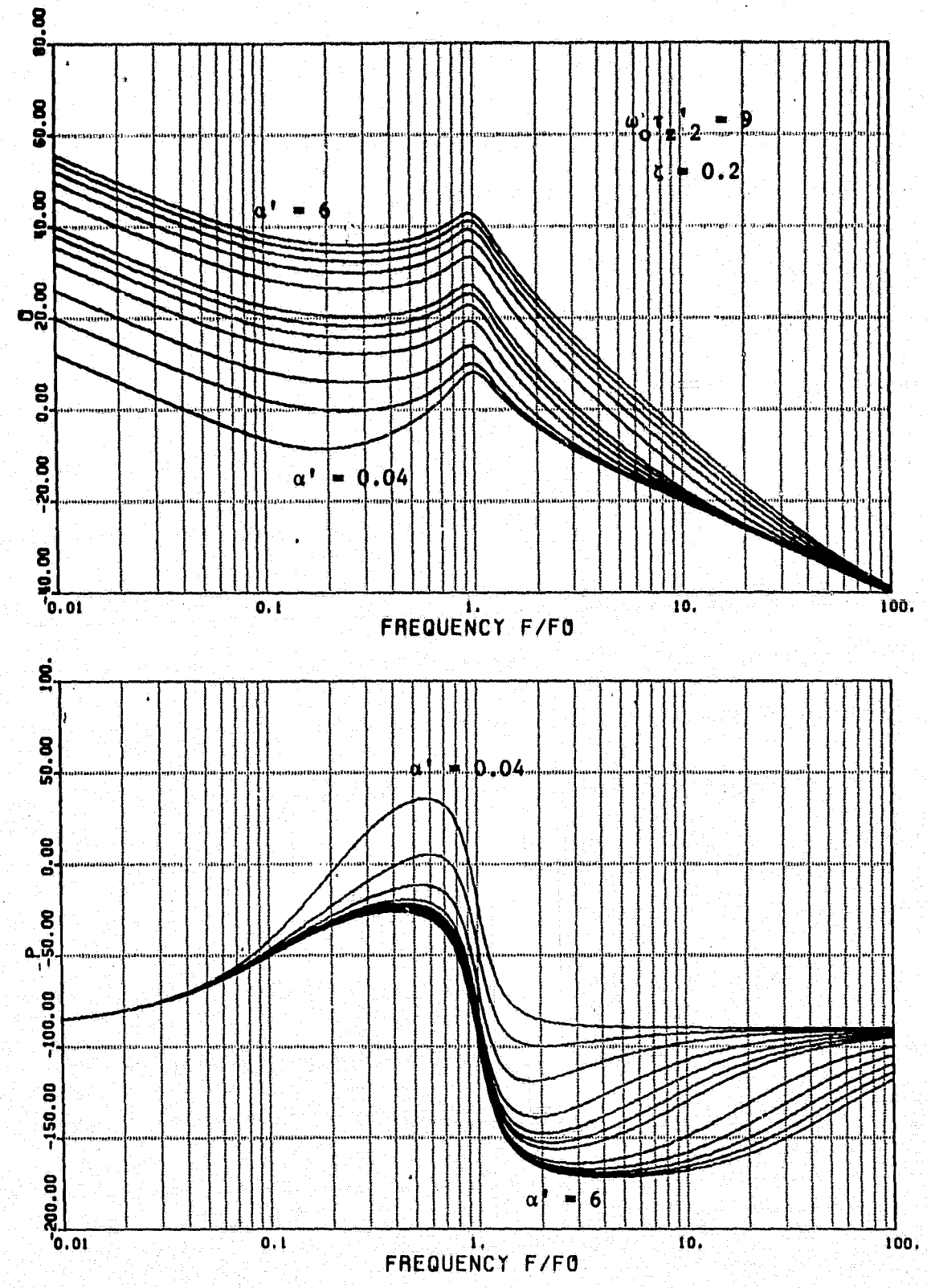
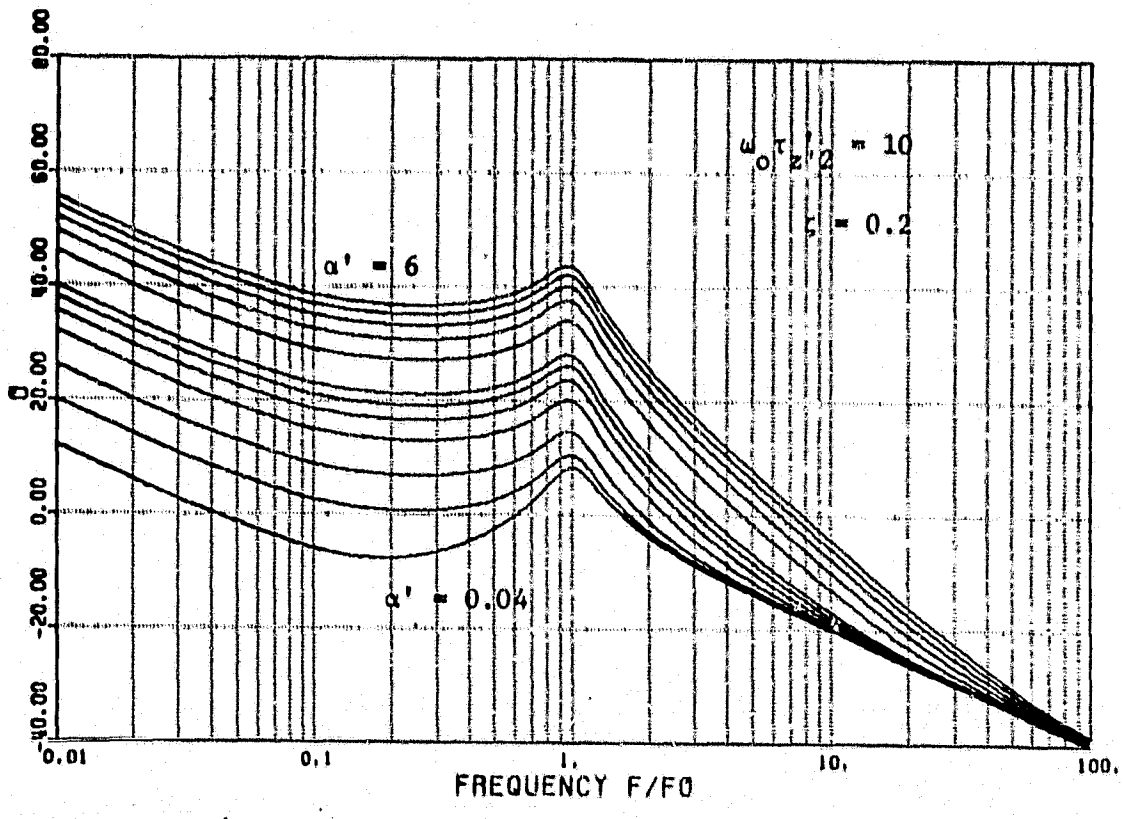


FIG. A.10 OPEN LOOP CHARACTERISTICS FOR $\omega_o \tau'_{z\,2} = 9$



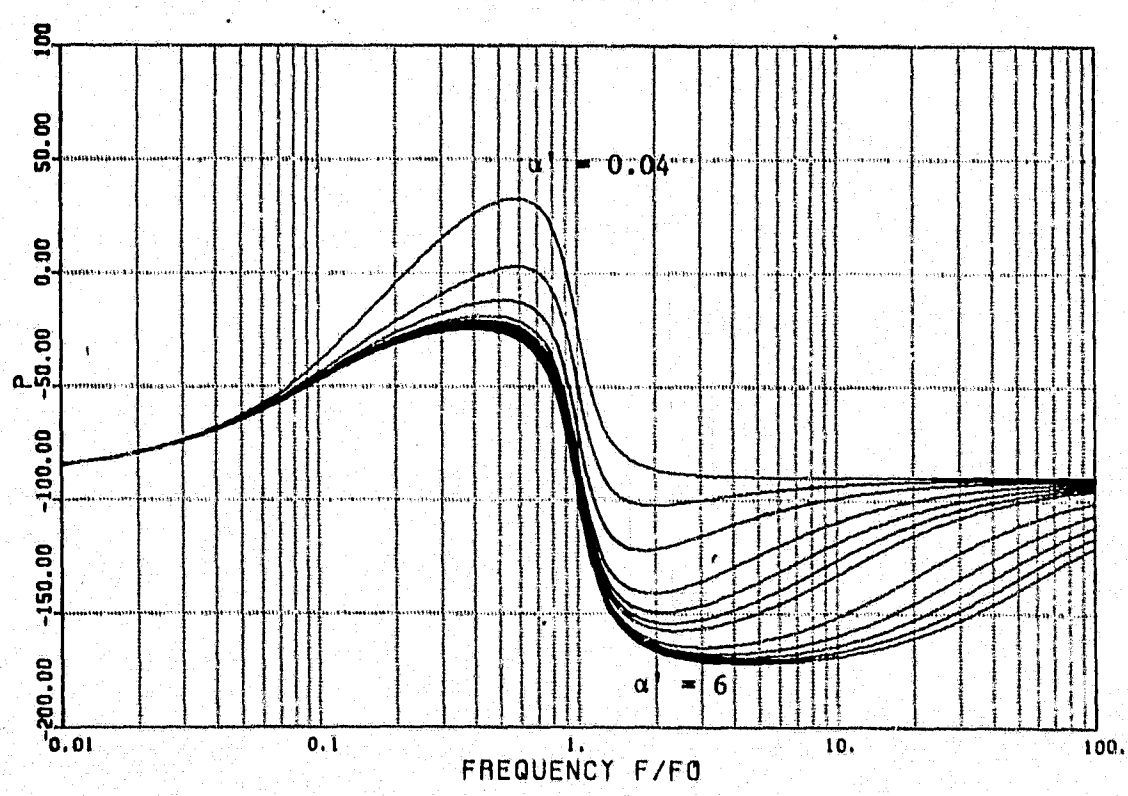


FIG. A.11 OPEN LOOP CHARACTERISTICS FOR $\omega_o \tau'_{z\,2} = 10$